STUDY OF NOVEL CHANNEL MATERIALS USING III-V COMPOUNDS WITH VARIOUS GATE DIELECTRICS

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ABSTRACT

The exponential rise in the density of silicon CMOS transistors has now reached a limit and threatening to end the microelectronics revolution. To tackle this difficulty, group III–V compound semiconductors due to their outstanding electron transport properties and high mobility are very actively being researched as channel materials for future highly scaled CMOS devices. In this paper, we have studied a ballistic nanoscale MOSFET using simulation approach by replacing silicon in the channel by III-V compounds. The channel materials considered are silicon (Si), Gallium arsenide (GaAs), Indium arsenide (InAs), Indium Phosphide (InP) and Indium Antimonide (InSb). The device metrics considered at the nanometer scale are subthreshold swing, Drain induced barrier lowering, on and off current, carrier injection velocity and switching speed. These channel materials have been studied using various dielectric constants. It has been observed that Indium Antimonide (InSb) has higher on current, higher transconductance, idealistic subthreshold swing, higher output conductance, higher carrier injection velocity and comparable voltage gain compared to Silicon, thus, making InSb as a possible candidate to be used as channel material in future nanoscale devices.

KEYWORDS

Channel materials, III-V compounds, Nanoscale MOSFETs.

1. INTRODUCTION

Latest International technology roadmap for semiconductors (ITRS) suggests that MOSFETs will reach sub-10 nm dimensions by 2016 [1]. However, to realize devices beyond the 45 nm technology node, novel device architectures along with high mobility materials are required for enhanced performances to improve the on-current and to reduce the power absorption [2-3]. Since the channel length has become comparable to the mean free path of the carriers in the inversion layer, the MOSFETs are expected to approach the ballistic transport mechanism and the ballistic current is affected by the channel material, wafer orientation and by the channel direction in the transport plane. I_{on} is given in terms of technological and channel material parameters by the following expression [4]:

$$I_{on} \propto \frac{8qh}{3\sqrt{\pi}} \frac{(N_{inv})^{\frac{3}{2}}}{(n_v)^{\frac{1}{2}}(m_W)^{\frac{1}{4}}(m_L)^{\frac{3}{4}}} \qquad (1)$$

where n_v is the valley degeneracy, while m_L and m_W are the effective masses in the direction of the channel length and width, respectively. The expression (1) reveals that the maximum I_{on} can be obtained for the smallest transport masses and valley degeneracy. Therefore, III-V compound semiconductors such as GaAs, InP, InAs, InSb etc., should be explored as alternative channel materials in the future nanoscale devices [5-6].

A high mobility channel material has high injection velocity to increase the on-state current and reduces delay. Currently, strained-Si is the dominant technology for high performance

MOSFETs and increasing the strain provides a viable solution to scaling. However, looking into future scaling of nanoscale MOSFETs, it is important to look at higher mobility materials, like Ge and III-V compounds together with innovative device structures and strain, which may perform better than even very highly strained Si. For both Ge and III-V devices, problems of leakage need to be solved. Due to their extremely small transport mass leading to high injection velocity (V_{inj}), III-V materials appear to be very attractive candidates as channel materials for highly scaled n-MOSFETs [7]. However, III-V materials have many significant and fundamental issues, which may prove to be severe bottlenecks to their implementation. Although their small transport mass leads to high V_{inj}, III-V materials have a low density of states (DOS) in the Γ-valley, tending to reduce the inversion charge (Q_{inv}) and hence reduce drive current [8-9]. Furthermore, the small direct band gaps of Ge and III-V materials inherently give rise to very large band to band tunneling (BTBT) leakage current compared to Si. Despite of low inversion charge (Q_{inv}), due to their large injection velocity (V_{inj}), III-V materials like InAs, InSb and InP can flow up to 80% larger drive current than Si. The $I_{OFF,\ BTBT}$ in Ge, InAs, GaAs and InSb can be reduced by over ~1000X by scaling.

Various heteroepitaxy approaches and structures for advanced channel material fabrication in "On-Insulator (OI)" structures using global and localized epitaxy techniques with strained-Si, Ge, III-V etc. have been suggested by Cheng [10]. OI architectures offer many technological advantages and improve both CMOS scalability and current drivability. In addition, OI architecture can help reducing the high leakage current associated with many advanced materials. Room temperature hole mobility in a 7.5nm thick Ge quantum well has already been reported to exceed 2500 cm^2/V-sec [11]. Recently, a great progress has been made to integrate high-k gate dielectric with Ge process and active research in this field is underway [12-15]. High performance, n- and p- channel Ge MOSFETs has been reported in [16-20]. Robust and highly manufacturable new process technologies, such as atomic layer deposition (ALD), heteroepitaxy and metal gates, have opened the opportunity to integrate III-V semiconductors with Si technology. With their exceptionally high mobilities, III-V materials display promise for ultra-fast, very low power digital logic technology. In [21-22], using ALD Al_2O_3 as the gate insulator, GaAs MOSFETs with excellent performance was reported for the first time. Later, GaAs MOSFET with oxidized InAlP gate insulator was reported in [23]. Other III-V materials, InAs and InSb, also show great promise as novel channel material for logic technology due to their exceptionally high carrier mobilities. InSb is a fascinating material because its high electron mobility is appropriate for high speed transistors and Hall-effect devices. Its narrow band gap is also suitable for infrared applications. InSb can be directly grown on Si substrate without insertion of buffer layer and leakage current between InSb and Si Substrate is very small. Recently, for the first time, InSb based Quantum Well FET has been reported [24]. Fischetti et al. showed in [8] that indium based semiconductors can outperform Si and Ge MOSFETs in deeply scaled MOSFETs.

The main aim of this paper is to provide an insight by replacing Silicon in the channel by III-V compound semiconductors using different dielectric constants. A comparison of InSb has been made with InP, InAs, GaAs and Si. Various channel materials used along with their properties are shown in Table 1 whereas various input parameters as well as dielectric materials used in the simulations are shown in tables 2 & 3 respectively.

Table 1. Cannel Materials used

		Compound Semiconductors			
	Si	**InP**	**GaAs**	**InAs**	**InSb**
Electron mobility (μ_n) Cm^2/v-s	1450	5900	9200	33000	77000
Effective mass	0.19	0.077	0.063	0.028	0.014
Band Gap (eV)	1.12	1.34	1.42	0.35	0.17
Valley degeneracy	2	1	1	1	1

Table 2. Parameters used for Simulation

S.No	**Input Parameters**	**Value**
1	Insulator thickness	5.00e-9
3	Temperature	300 K
4	Threshold voltage	0.32 ev
5	Gate control parameter	1.00
6	Drain control	0
7	Voltage Loop (for both Vgs & Vds)	Initial Bias =0 V Final Bias=1.0V

Table 3. Dielectric Materials used

Dielectric Materials used	**Dielectric Constant (k)**
SiO_2	3.9
Si_3N_4	7.5
HfO_2	20
ZrO_2	25

2. SIMULATION RESULTS AND DISCUSSIONS

Figure 1 shows the structure of the simulated device. Various parameters used for the simulation are as listed in tables 1, 2 and 3. In this section we will discuss various simulation results obtained.

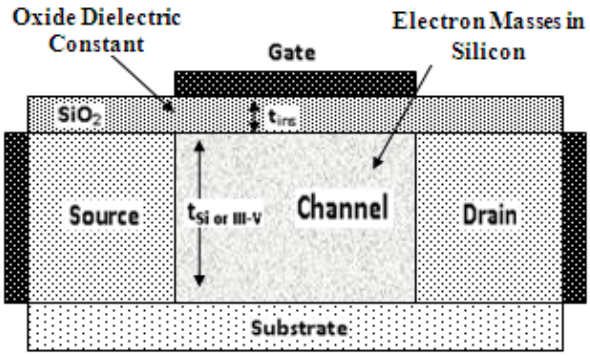

Figure 1. Structure of the proposed device

Figure 2 shows the I_{ds}-V_{ds} characteristics for different dielectrics at constant V_{gs} = 1V, t_{ins} = 5nm and InSb as channel material. Exact saturation occurs around 0.4V to 0.6V for all the dielectric materials. ZrO_2 has a high saturation voltage around 0.6V with highest saturation current. This figure further indicates that drain current increases with increase in drain voltage upto pinch-off voltage and beyond this point there is no effect of drain voltage over the drain current as happens in conventional MOSFETs.

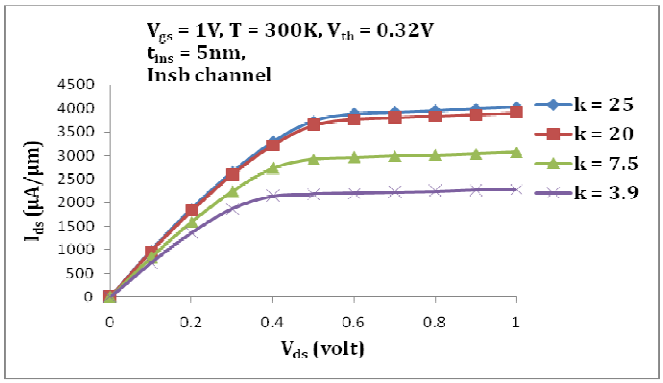

Figure 2. I_{ds} –V_{ds} characteristics

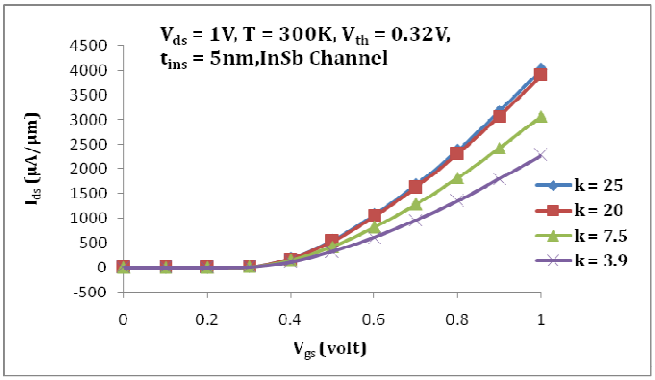

Figure 3. I_{ds}-V_{gs} Characteristics

Figure 3 shows the I_{ds}-V_{gs} characteristics for different dielectrics at constant V_{ds} = 1V, t_{ins} = 5nm and InSb as channel material. ZrO_2 has higher drain currents but requires lower threshold voltage. Thus, it is not possible to suppress subthreshold effects and quantum confinement cannot be achieved.

Figure 4 shows the quantum capacitance vs. gate voltage behavior for various dielectrics and InSb as channel material. The device can be operated at quantum capacitance limit when its gate capacitance is considerably higher than quantum capacitance. To know device operation at QCL limit, value of quantum capacitance at inversion, depletion accumulation region of the device,

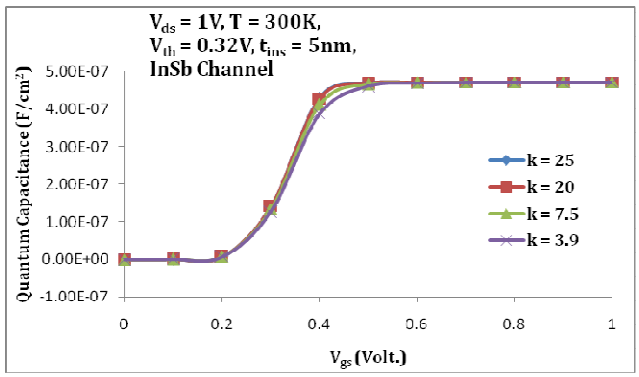

Figure 4. Variation of Quantum Capacitance w. r. t. gate voltage for different dielectrics.

the study of Qc – V_g curves is necessary. For ZrO_2 at low voltage (upto V_g = 0.2V) quantum capacitance remains constant. SiO_2 has low quantum capacitance. ZrO_2 has well defined accumulation and inversion regions with higher threshold voltage due its higher gate capacitance and quantum capacitance.

Figure 5 shows transconductance/drain current ratio (g_m/I_d) variations w. r. t. gate voltage for different dielectrics at constant V_{ds} = 1V and t_{ins} = 5nm and InSb as channel material. As the V_{gs} increases, the g_m/I_d decreases, in other words, the sensitivity of the device (g_m) by governing the equation, $g_m = I_d/V_{gs}$. As we know that the maximum performance is obtained when the value of g_m/I_d ratio also known as transconductance efficiency is the largest. ZrO_2 has slightly higher value of g_m/I_d ratio than the other dielectric materials.

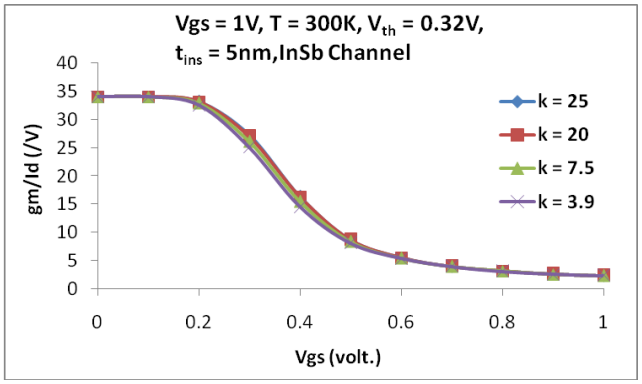

Figure 5. Variations of gm/Id w. r. t. gate voltage for different dielectrics.

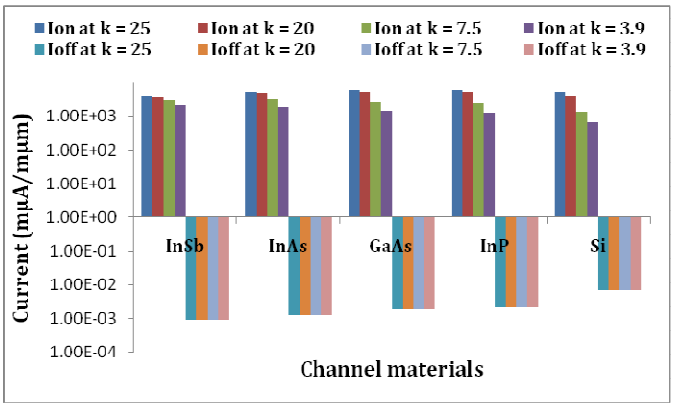

Figure 6: I_{on} and I_{off} for different channel materials.

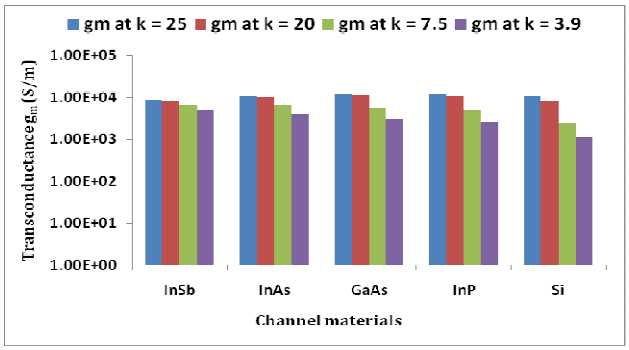

Figure 7: g_m for different channel materials.

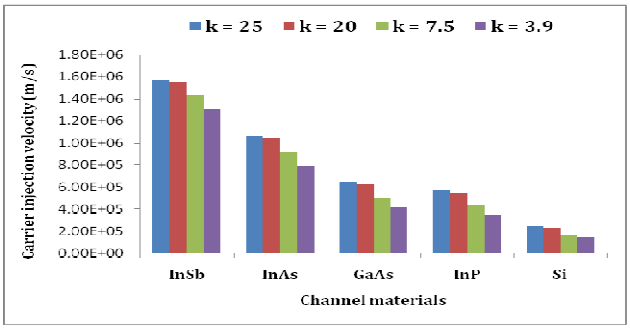

Figure 8: V_{inj} for different channel materials.

The bar graph in Figure 6 indicates that InSb has lowest I_{off} and highest I_{ON} current among other channel materials at various dielectrics. The switching speed (I_{on}/I_{off} ratio) is highest for InSb. Figure 7 suggests that InSb has higher transconductance than other channel materials for different dielectrics. Further, Figure 8 suggests that the carrier injection velocity or in other words, mobility of charge carriers in InSb is higher compared to the other channel materials for different dielectrics which give higher I_{on} current.

3. CONCLUSIONS

Based on the various results obtained, we conclude that InSb has higher on-current, lowest off-current for ZrO_2 as dielectric material. It means the nanoscale MOSFET has fast switching speed. It has maximum carrier injection velocity due to high mobility and high current handling capability with low gate derives voltage for achieving high frequency response. It has subthreshold swing of 59.70 mV/decade (very close to practical value i.e. 60 mV/decade), and highest than other channel materials. Hence, we can say that InSb channel material enhance the device performance and could be used as novel channel material in future nanoscale devices.

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