

Performance Analysis of Gate Misaligned Triple Material Double Gate (TMDG) MOSFET

R.Divyabharathy¹, C.Vinoliya Cathrin¹,
S.Pandi priya¹

¹UG Student, Dept. of ECE, VCET, Madurai

ABSTRACT

In the literature, the misalignment effects in a nanoscale MOSFET is analyzed for dual material Double gate MOSFET. The analysis is used in the design criterion of the device. In this paper, a two dimensional analytical model of gate misalignment effects in Triple Material Double Gate (TM-DG) MOSFET is presented for the first time. The gate misalignment effect in the drain side is considered. Based on the misaligned gate, the device is split in to six regions. The boundary conditions are obtained considering the electric flux and the potential. The parameters are derived using region based approach. Parameters like surface potential and electric field is studied. In general various methods like superposition method, Fourier series method, Numerical methods are used to analyze the device. In our paper, the parabolic approximation method is used for analytical modeling of TM-DG MOSFET since it is more accurate than the other methods available in the literature. The results are simulated and compared with dual material double gate MOSFET. The device performance is analyzed and it helps in the design scenario.

KEYWORDS

Triple Material Double Gate (TM-DG) MOSFET, short channel effect (SCE), Gate misalignment, Surface potential.

1. INTRODUCTION

For the past few years, scaling of devices has been a great advancement in the field of Very Large Scale Integration(VLSI).As MOSFETs are scaled to 100nm, effects such as short channel-effect(SCE), drain induced barrier lowering(DIBL), hot carrier effect etc. occurs[1][2]. As a result of short channel effect, the control gets transferred from gate to drain[3]. To overcome this effect, multigate MOSFETs are probably used. There are different types of multigate MOSFETs. Some of them are Double Gate (DG), Triple Gate (TG), Quadruple Gate (QG), Cylindrical Gate (CG), Independent Gate, Bulk FinFET.

In double gate MOSFET there are two gates, front gate and back gate. The presence of two gates in DG MOSFET helps to minimize the short channel effects when compared to single gate. The introduction of gate engineering in DG MOSFETs still reduces the short channel effects to the minimum. Gate engineering is one of the important technique in which the gate of the MOSFET is made of different materials [4]. Depending on the number of material used in the gate, gate engineering is divided into single gate material, dual gate material and triple gate material. A two-dimensional analytical modeling and simulation of Dual-material Double gate (DM-DG) nanoscale SOI MOSFET is proposed [5]. It concludes that, it exhibits significantly reduced short-channel effects (SCE) when compared with the DG SOI MOSFET and further, model for the drain current, transconductance, drain conductance, and voltage gain is also discussed[5]. Pramod Kumar Tiwari and Sarvesh Dubey has proposed a two-dimensional analytical model for threshold voltage of short-channel Triple-material Double-gate (TM-DG) MOSFET[6]. TM-DG MOSFET

is superior to DM-DG MOSFET in terms of screening these effects, since the number of material increases. The technique used to screen the short channel effect is to make the step-function of the surface potential. The step shape can be achieved by using more than one material of different work function[7]. In spite of several benefits, there are some issues affecting the eventual circuit performance. Among them the most important one is misalignment between the front and back gate. The misalignment can be considered either in the drain side or source side. Due to misalignment, the device properties such as surface potential, threshold voltage, drain current gets affected[8]. There are many methods like superposition method, Fourier series method to analyze the device. Elvis C.Sun and James B.Kuo has analyzed the effect of surface potential, threshold voltage due to gate misalignment in a Single Material Double Gate(SM-DG) MOSFET considering fringing electric field by using conformal mapping method[9]. Rupendra Kumar Sharma and Rithesh Gupta has proposed a structure on gate misaligned Dual Material Double Gate(DM-DG) SOI n-MOSFET and the effect on surface potential, threshold voltage, DIBL variation, subthreshold-slope variation, sub-threshold drain-current, transconductance are observed. So far analysis is done only for single material(SM) and double material (DM) Double Gate (DG) MOSFET[10]. In this paper, an analysis of the gate misalignment effect on surface potential of Triple Material Double Gate(TM-DG) MOSFET is reported using region based parabolic approximation method. In this method, the device is divided into regions based on the overlapping and non-overlapping region.

2. PROPOSED STRUCTURE

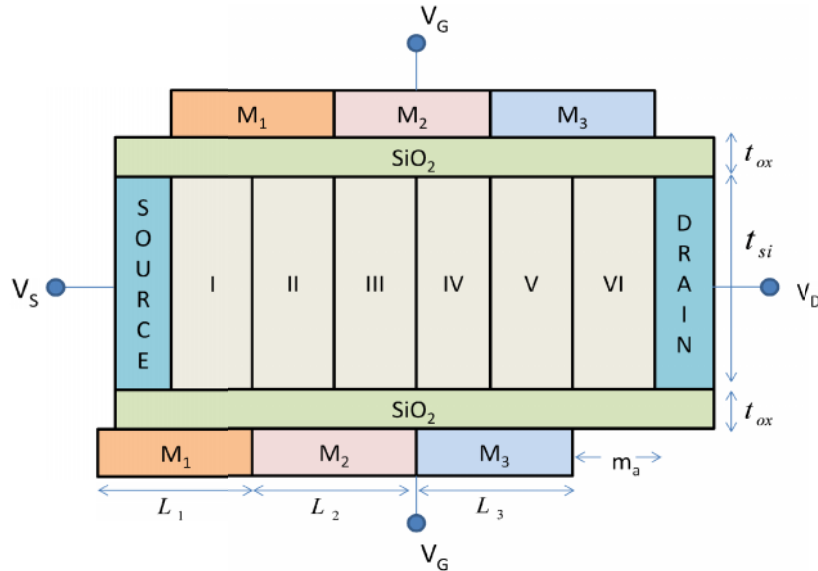


Figure 1: Schematic view of Gate Misaligned TM-DG MOSFET

The basic structure of drain side misaligned Triple material Double gate(TM-DG) MOSFET is shown in fig 1. The gate consists of three materials (M_1 , M_2 , M_3) each of length L_1 , L_2 , L_3 , and their work functions are ϕ_{M1} , ϕ_{M2} , ϕ_{M3} . The gate length L is given by $L=L_1+L_2+L_3$. The material near the source has higher work function (ϕ_{M1}), the middle material has intermediate work function (ϕ_{M2}) and the material with lower work function (ϕ_{M3}) is placed near the drain. M_1 is known as control gate and M_2 , M_3 are known as screening gate. t_{si} is the channel thickness which varies from 30nm to 90nm and t_{ox} is the gate oxide thickness which varies from 1nm to 5nm. The analysis has been performed by splitting the channel into 6 regions based on overlap and non-

overlap region. In region I, III and V both the front and the back gate consists of same material. So, they are non-overlap region. Region II, IV and VI are called overlap region since, it consists of different materials.

3. MODEL DERIVATION

The 2-D surface potential distribution for all the six regions can be obtained by using the 2-D poisson's equation along with appropriate boundary conditions.

$$\frac{\partial^2 \phi(x, y)}{\partial x^2} + \frac{\partial^2 \phi(x, y)}{\partial y^2} = \frac{qN_a}{\epsilon_{si}} \quad (1)$$

Where ϵ_{si} is the silicon permittivity, q is the electronic charge, and $\phi(x,y)$ is the 2-D surface potential distribution in the silicon film.

The boundary conditions for front gate for six regions are given by,

$$\frac{\partial \phi_j(x, y)}{\partial y} \Big|_{y=0} = \frac{C_{ox}}{\epsilon_{si}} [\phi_{sj}(x) - V_G + Vfb_{fj}] \quad (2)$$

The boundary condition for back gate for five regions are given by,

$$\frac{\partial \phi_j(x, y)}{\partial y} \Big|_{y=tsi} = \frac{C_{ox}}{\epsilon_{si}} [V_G - Vfb_{bj} - \phi_{bj}(x)] \quad (3)$$

For sixth region

$$\frac{\partial \phi_j(x, y)}{\partial y} \Big|_{y=tsi} = \frac{\epsilon_{ox}}{\epsilon_{si}t(x)} [V_G - V_{fbb4} - \phi_{b4}(x)] \quad (4)$$

Where the flatband voltage of front and back gate are,

$$Vfb_{bj} = \phi_{Mj} - \phi_s \quad Vfb_{fj} = \phi_{Mj} - \phi_s \quad (5)$$

Where ϕ_{Mj} - material work function and j varies with respect to the materials used. The

semiconductor work function is given by $\phi_s = \chi_s + \left(\frac{E_g}{2}\right) + \phi_t$ where $\phi_t = \left(\frac{kT}{q}\right) \ln\left(\frac{N_A}{n_i}\right)$ is the bulk potential, E_g is the silicon band gap, and χ_s is the electron affinity.

3.1. Front Side Surface Potential

The potential will be continuous throughout the channel region and electric flux will be continuous at the interfaces. Hence the boundary condition for the interfaces II-III and IV-V are

$$\begin{aligned} \text{Potential:} \quad & \phi_2(L_1, 0) = \phi_3(L_2, 0) \\ & \phi_4(L_1 + L_2, 0) = \phi_5(L_1 + L_2, 0) \end{aligned} \quad (6)$$

Electric flux:
$$\frac{\partial \phi_2(x, y)}{\partial x} \Big|_{x=L_1} = \frac{\partial \phi_3(x, y)}{\partial x} \Big|_{x=L_1} \tag{7}$$

$$\frac{\partial \phi_4(x, y)}{\partial x} \Big|_{x=L_1+L_2} = \frac{\partial \phi_5(x, y)}{\partial x} \Big|_{x=L_1+L_2}$$

Potential at source end:
$$\phi_1(0,0) = \phi_{s1}(0) = V_{bi} \tag{8}$$

Potential at drain end:
$$\phi_3(L_1 + L_2 + L_3, 0) = \phi_{s3}(L_1 + L_2 + L_3) = V_{bi} + V_{DS} \tag{9}$$

Where $v_{bi} = v_T \ln \left(\frac{N_a N_{DS}}{n_i^2} \right)$ (10)

By using parabolic approximation method the solution for Poisson equation is obtained as

$$\phi_j(x, y) = a_{j0}(x) + a_{j1}(x)y + a_{j2}(x)y^2 \tag{11}$$

By using the boundary conditions (2), (3), (5), (6) to (11) along with equation (1) the front surface potential $\phi_{sj}(x)$ for the six regions are obtained as

$$\phi_{Cj}(x) = A_j \exp(\eta x) + B_j \exp(-\eta x) - \frac{\beta_j}{\alpha}; j = 1, 2, 3 \tag{12}$$

On considering only the front gate, since there is no misalignment the regions can be clubbed together based on the gate material. Region I and II can be considered together as it consists of same gate material. The same lies for the other region III and IV, V and VI. Hence j varies from 1 to 3.

$$A_1 = \frac{V_{bi} + V_{DS} + \frac{\beta_3}{\alpha} - (V_{bi} + \frac{\beta_1}{\alpha}) \exp[\eta(L_1 + L_2 + L_3)] + \frac{(\beta_1 - \beta_2)}{\alpha} \cosh[\eta(L_2 + L_3)] + \frac{(\beta_2 - \beta_3)}{\alpha} \cosh(\eta L_3)}{2 \sinh[\eta(L_1 + L_2 + L_3)]} \tag{13}$$

$$B_1 = V_{bi} + \frac{\beta_1}{\alpha} - A_1 \tag{14}$$

$$A_2 = A_1 \exp(\eta L_1) - \frac{(\beta_1 - \beta_2)}{2\alpha} \tag{15}$$

$$B_2 = (V_{bi} + \frac{\beta_1}{\alpha} - A_1) \exp(-\eta L_1) - \frac{(\beta_1 - \beta_2)}{2\alpha} \tag{16}$$

$$A_3 = A_1 \exp[\eta(L_1 + L_2)] - \frac{(\beta_1 - \beta_2)}{2\alpha} \exp(\eta L_2) - \frac{(\beta_2 - \beta_3)}{2\alpha} \tag{17}$$

$$B_3 = \left(V_{bi} + \frac{\beta_1}{\alpha} - A_1 \right) \exp[-\eta(L_1 + L_2)] - \frac{(\beta_1 - \beta_2)}{2\alpha} \exp(-\eta L_2) - \frac{(\beta_2 - \beta_3)}{2\alpha} \quad (18)$$

$$\beta_j = \frac{qN_a}{\epsilon_{si}} - \frac{V_{GS} - V_{fbj}}{\lambda^2} \quad \frac{1}{\lambda^2} = \frac{2r}{t_{si}^2 \left(1 + \frac{r}{4} \right)} \quad \eta = \frac{1}{\lambda} = \sqrt{\alpha} \quad (19)$$

3.2. Back Side Surface Potential

The boundary conditions for the interfaces I-II, III-IV and V-VI are

$$\begin{aligned} \text{Potential:} \quad \phi_1\left(\frac{L_1}{2}\right) &= \phi_2\left(\frac{L_1}{2}\right) \\ \phi_3\left(\frac{L_1}{2} + L_2\right) &= \phi_4\left(\frac{L_1}{2} + L_2\right) \\ \phi_5\left(L_1 + L_2 + \frac{L_3}{2}\right) &= \phi_6\left(L_1 + L_2 + \frac{L_3}{2}\right) \end{aligned} \quad (20)$$

$$\begin{aligned} \text{Electric flux:} \quad \frac{\partial \phi_1(x)}{\partial x} \Big|_{x=\frac{L_1}{2}} &= \frac{\partial \phi_2(x)}{\partial x} \Big|_{x=\frac{L_1}{2}} \\ \frac{\partial \phi_3(x)}{\partial x} \Big|_{x=\frac{L_1}{2} + L_2} &= \frac{\partial \phi_4(x)}{\partial x} \Big|_{x=\frac{L_1}{2} + L_2} \\ \frac{\partial \phi_5(x)}{\partial x} \Big|_{x=L_1 + L_2 + \frac{L_3}{2}} &= \frac{\partial \phi_6(x)}{\partial x} \Big|_{x=L_1 + L_2 + \frac{L_3}{2}} \end{aligned} \quad (21)$$

$$\text{Potential at source end:} \quad \phi_1(0,0) = \phi_{s1}(0) = V_{bi} \quad (22)$$

$$\text{Potential at drain end:} \quad \phi_3(L_1 + L_2 + L_3, 0) = \phi_{s3}(L_1 + L_2 + L_3) = V_{bi} + V_{DS} \quad (23)$$

Where $v_{bi} = v_T \ln\left(\frac{N_a N_{DS}}{n_i^2}\right)$ (24)

By using parabolic approximation method the solution for Poisson equation is obtained as

$$\phi_j(x, y) = a_{j0}(x) + a_{j1}(x)y + a_{j2}(x)y^2$$
 (25)

By using the boundary conditions (2) to (5), (20) to (25) along with equation (1) the back surface potential $\phi_{bj}(x)$ for the six regions are obtained as

$$\phi_{sj}(x) = A_j \exp(kx) + B_j \exp(-kx) - \frac{m_j}{k^2}; j=1 \text{ to } 6$$
 (26)

$$\left. \begin{aligned}
 p_1 &= \frac{p}{\left(2 \sinh\left(k\left(L_1 + L_2 + \frac{L_3}{2}\right)\right)\right) - \left(\frac{(k+k_1)}{2k_1 \exp\left(-k\left(L_1 + L_2 + \frac{L_3}{2}\right)\right)}\right) + \left(\frac{(k_1-k)}{2k_1 \exp\left(k\left(L_1 + L_2 + \frac{L_3}{2}\right)\right)}\right)} \\
 p_2 &= \frac{p}{-\left(\frac{(k_1-k)}{2k_1 \exp\left(k_1\left(\frac{L_3}{2}\right)\right) \exp\left(k\left(L_1 + L_2 + \frac{L_3}{2}\right)\right)}\right) + \left(\frac{(k_1+k)}{2k_1 \exp\left(-k\left(\frac{L_3}{2}\right)\right) \exp\left(-k\left(L_1 + L_2 + \frac{L_3}{2}\right)\right)}\right)} \\
 a_1 &= p_1 + p_2 & b_1 &= V_{bi} + \frac{m_1}{k^2} - a_1 & a_2 &= \frac{2k^2 a_1 \exp\left(k\left(\frac{L_1}{2}\right)\right) - m_1 + m_2}{2k^2 \exp\left(k\left(\frac{L_1}{2}\right)\right)} \\
 b_2 &= \frac{w - a_1 \exp\left(-k\left(\frac{L_1}{2}\right)\right)}{\exp\left(-k\left(\frac{L_1}{2}\right)\right)} & a_3 &= \frac{2ka_1 \exp\left(k\left(\frac{L_1}{2}\right)\right) - m_1 + m_2 - \left(m_2 - m_3\right) \exp\left(-k\left(\frac{L_1}{2}\right)\right)}{2k \exp\left(k\left(\frac{L_1}{2}\right)\right)} \\
 b_3 &= v \exp(kL_1) - a_1 & a_4 &= a_1 + u & b_4 &= -a_1 + t
 \end{aligned} \right\} (27)$$

$$\left. \begin{aligned}
 a_5 &= a_1 - \left(\frac{m_4 - m_5}{2k^2 \exp(L_1 + L_2)} \right) + u & b_5 &= -a_1 + s \\
 p_3 &= \frac{2a_1(k + k_1)}{2k_1 \exp\left((k + k_1)\left(L_1 + L_2 + \left(\frac{L_3}{2}\right)\right)\right)} - \frac{a_1(k_1 - k)}{2k_1 \exp\left((k + k_1)\left(L_1 + L_2 + \left(\frac{L_3}{2}\right)\right)\right)} \\
 p_4 &= \frac{r_1}{2k_1 \exp\left(k_1\left(L_1 + L_2 + \frac{L_3}{2}\right)\right)} \\
 p_5 &= \frac{q_1}{\exp\left(-k\left(L_1 + L_2 + \left(\frac{L_3}{2}\right)\right)\right)} + \frac{a_1(k_1 - k)}{2k_1 \exp\left(-k_1\left(\frac{L_3}{2}\right)\right) \exp\left((k - k_1)\left(L_1 + L_2 + \left(\frac{L_3}{2}\right)\right)\right)} \\
 p_6 &= -\frac{a_1(k_1 + k)}{2k_1 \exp\left(-k_1\left(\frac{L_3}{2}\right)\right) \exp\left(-(k + k_1)\left(L_1 + L_2 + \left(\frac{L_3}{2}\right)\right)\right)} \\
 a_6 &= p_3 + p_4 & b_6 &= p_5 + p_6
 \end{aligned} \right\} (28)$$

4. RESULTS AND DISCUSSION

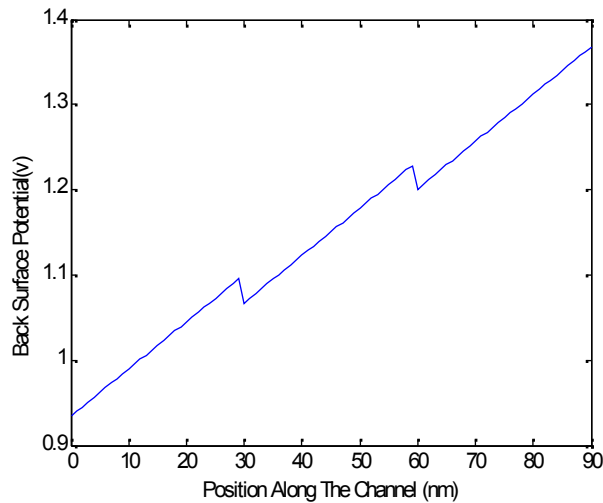


Figure 2. Front Surface Potential

The figure 2 demonstrates how the short channel effects are reduced in gate engineering and it also depicts the change in the surface potential due to misalignment in the gate .In figure, two step ups are observed in the potential. This is due to the screening of short channel effects that occurs due to the interface of different materials. The gate materials used are of three different materials which have different work function. The gate materials are arranged in such a way that the material with the highest work function is placed in the source side and the material with the lowest work function is placed at the drain side. The first step up shows the gate material2 screens the material1 from short channel effects. Similarly the second step up still preserves the material2 from SCEs. This also reduces the short channel effects due to Drain Induced Barrier Lowering(DIBL).When the drain voltage is increased, it causes change only in the drain side and the source side remains unaffected. This shows the reduction of short channel effects.

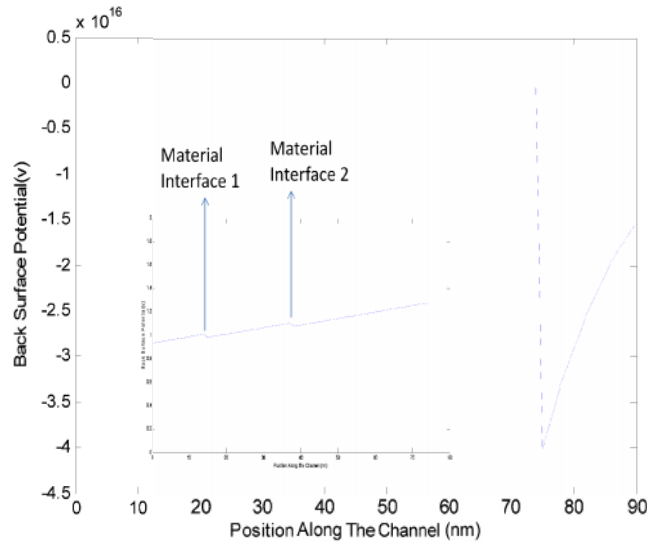


Figure 3. Back Surface Potential

Figure 3 shows the change in surface potential due to gate misalignment. Due to misalignment, the surface potential gets reduced from source to drain side. The minimum of the surface potential increases with an increase in the misalignment and barrier height reduces. A stepdown occurs at misaligned length which indicates the decrease in surface potential. Due to this, the short channel effect (SCE) and Drain Induced Barrier Lowering are reduced.

5. CONCLUSION

The effect of gate misalignment in Triple material Double gate (TM-DG) MOSFET has been examined by developing an analytical surface potential model by using MATLAB simulation. Though TM-DG is superior to other devices i.e. screening of short channel effect, increased surface potential etc, the gate misalignment degrades the device performance. As there is no misalignment, the profile surface potential shows a step shape, which reduces the short channel effect. With the increase in gate misalignment, the surface potential decreases. The performance analysis of misaligned TM-DG MOSFET helps in the design criterion of the device.

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Authors

R.Divyabharathy was born on 11.07.1993.She pursues final year B.E in Velammal College of Engineering and Technology, Madurai. Her research areas include device modeling and analog VLSI design



S.Pandi Priya was born on 09.12.1992. She pursues final year B.E in Velammal College of Engineering and Technology, Madurai. Her research area includes micro electronics and device modeling.



C.Vinoliya Cathrin was born on 18.09.1992. she pursues final year B.E in Velammal College of Engineering and Technology, Madurai. Her research area includes nano electronics and MOSFET devices

