FIXED WIDTH BOOTH MULTIPLIER BASED ON PEB CIRCUIT

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ABSTRACT

In this brief, a probabilistic estimation bias (PEB) circuit for a fixed-width two's complement Booth multiplier is proposed. The proposed PEB circuit is derived from theoretical computation, instead of exhaustive simulations and heuristic compensation strategies that tend to introduce curve-fitting errors and exponential-grown simulation time. Consequently, the proposed PEB circuit provides a smaller area and a lower truncation error compared with existing works. Implemented in an 8 × 8 2-D discrete cosine transform (DCT) core, the DCT core using the proposed PEB Booth multiplier improves the peak signal-to-noise ratio by 17 dB with only a 2% area penalty compared with the direct-truncated method.

Index Terms

Discrete cosine transform (DCT), estimation theory, fixed-width Booth multiplier, probabilistic analysis.

I. INTRODUCTION

FIXED-WIDTH multipliers generate an output with the same width as the input. They are widely used in digital Signal processing systems, such as discrete cosine transform (DCT), finite-impulse-response filter(FIR), and fast Fourier transform(FFT). Nevertheless, the computation error is introduced if the least significant (LS) half part is directly truncated. To reduce the computation error, many compensation techniques were presented for array multipliers. There is an apparently tradeoff between accuracy and hardware complexity. Recently, compensation works have been increasing, focused on reducing the truncation error on the Booth multiplier. In, Jou *et al.* have presented statistical and linear regression analysis to reduce the hardware complexity. However, the truncation error was partly depressed because the estimating

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information that came from the truncated part is limited. Song *et al.* determined the estimation threshold by using a statistical analysis. Huang *et al.* have presented a self compensation approach using a conditional mean derived from exhaustive simulation. Nevertheless, these time-consuming exhaustive simulations and heuristic compensation strategies may introduce curve fitting errors. Heuristic compensation bias circuits can reduce the error further by using more inputs from the encoder; however, these circuits consume more hardware overhead.

This study proposes a probabilistic estimation bias (PEB) method for reducing the truncation error in a fixed-width Booth multiplier. The PEB formula is derived from the probabilistic analysis in the partial
product array after the Booth encoder. In addition, the low-error and area-efficient PEB circuit is

TABLE I : MODIFIED BOOTH ENCODER AND PROBABILITIES OF THE ENCODED WORD

Y_{2i+1}	Y_{2i}	Y_{2i-1}	Y'_i	$P\{Y'_O\}$	$P\{Y'_i\}$
1	1	1	0	0	2/8
0	0	0	0	1/4	
0	0	1	1	0	2/8
0	1	0	1	1/4	
0	1	1	2	0	1/8
1	0	0	-2	1/4	
1	0	1	-1	0	2/8
1	1	0	-1	1/4	

obtained based on the simple and systematic procedure. In this way, the time-consuming exhaustive simulation and the heuristic design process of the compensation circuit can be avoided. Furthermore, the hardware efficiency and low error are validated through our simulation results.

II. FIXED-WIDTH BOOTH MULTIPLIER

Modified Booth encoding is popular to reduce the number of partial products. Two L-bit inputs X and Y, and a $2L$-bit standard product SP (without truncation error) can be expressed in two's complement representation as follows:

$$X=-x_{L-1}.2^{L-1}+\sum_{i=0}^{L-2} X_i.2^i$$

$$Y=-y_{L-1}.2^{L-1}+\sum_{i=0}^{L-2} Y_i.2^i$$

$$SP = X \times Y. \quad (1)$$

The modified Booth encoder maps three concatenated inputs y_{2i+1}, $y2_i$, and y_{2i-1} into y'_i, which are tabulated in Table I,where $P\{y'_i\}$ stands for the probability of y'_i. After encoding, there are $Q = L/2$ rows in the partial product array with an even width L. The corresponding partial products

represented in input x_i are tabulated in Table II, where the last column n_i stands for the sign of each partial product.

Table II : PARTIAL PRODUCTS FOR EACH BOOTH ENCODER

Y'_i	$P_{10,i}$	$P_{9,i}$	$P_{8,i}$	$P_{7,i}$	$P_{6,i}$	$P_{5,i}$	$P_{4,i}$	$P_{3,i}$	$P_{2,i}$	$P_{1,i}$	$P_{0,i}$	n_i
0	0	0	0	0	0	0	0	0	0	0	0	0
1	X_9	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	0
-1	X'_9	X'_9	X'_8	X'_7	X'_6	X'_5	X'_4	X'_3	X'_2	X'_1	X'_0	1
2	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	0	0
-2	X'_9	X'_8	X'_7	X'_6	X'_5	X'_4	X'_3	X'_2	X'_1	X'_0	1	1

An example of 10 × 10 fixed-width Booth multiplier with the Booth encoder is displayed in Fig. 1. The partial product array can be divided into two parts: the main part (MP), which includes ten most significant columns (MSCs), and the truncation part (TP), which includes ten LS columns (LSCs). The SP can be rewritten as follows:

$$SP = MP + TP. \qquad (2)$$

In the fixed-width multiplication, TP can be estimated and the quantized product QP can be defined as

$$QP = MP + \sigma .2^L \qquad (3)$$

where σ representing the estimation bias (EB) from TP can be further decomposed into TPMajor (MSC of TP) and TPminor (LSCs of TP) parts as

$$\sigma = \text{Round}\left(\frac{1}{2}\ \text{TPMajor} + \text{TPminor}\right) \qquad (4)$$

$$\text{TPMajor} = \sum_{j=0}^{Q-1} P_{L-1-2j,j} \qquad (5)$$

$$\text{TPminor} = \text{TP}m1 + \text{TP}m2 \qquad (6)$$

where Round(k) is rounding k to the nearest integer. In Fig. 1, because TPMajor affects more than TPminor while contributing toward the EB σ, the σ value can be obtained by calculating TPMajor and estimating TPminor in order to reduce truncation errors. In our analysis of estimation, expected values on all elements including n_i in TPminor are derived. First, we derive the expected values (probabilities of being one) on all elements in TPminor, except for $P_{0,0}$ and n_0. Taking column $P_{0,i}$ (i '= 0) in Table II as an example, we sum up the expected values on nonzero terms in the third, fourth, and sixth rows. When the third row (y'_i = 1) is taken into consideration, the expected value of x_0 is 1/2 because the probability of each input bit is assumed to be uniformly distributed. Then, we can trace back to Table I and find that probability $P\{y'_i = 1\}$ is 2/8. It is straightforward to compute the expected value of $P_{0,i}$ ($i \neq 0$) to be

$$E[P_{0,i}]=\sum_{k=\{1,-1,2,-2\}} P\{P_{0,i}=1|y_i'=k\}.P\{y_i'=k\}$$

$$=\frac{1}{2}*\frac{2}{8}+\frac{1}{2}*\frac{2}{8}+0*\frac{1}{8}+1*\frac{1}{8}=\frac{3}{8}$$

Similarly, the expected value $E[n_i]$ is equal to 3/8. Second, when we calculate the expected values of $E[P_{0,0}]$ and $E[n_0]$ in the LSC of TPminor, only four conditions marked as gray rows in Table I occur. The expected value $E[P_{0,0}]$ can be derived as follows:

$$E[P_{0,0}] =\sum_{k=\{1,-1,-2\}} P\{P_{0,0}=1|_{yi'=k}\}.P\{y_i'=k\}$$

	L=8	L=10	L=12	L=16	L=32
3L/32	0.75	0.9375	1.125	1.5	3
A	0	0	1	1	3
B	1	1	0	1	0

$$=\frac{1}{2}*\frac{1}{4}+\frac{1}{2}*\frac{1}{4}+1*\frac{1}{4}=\frac{1}{2} \qquad (8)$$

Similarly, the expected value $E[n_0]$ is 1/2 as well. Hence, the expected values of all elements (including n_i) in TPminor are obtained as follows:

Case 1: Elements in the LSC

$$E[P_{0,0}] =1/2== E[n_0]. \qquad (9)$$

Case 2: Other elements

$$E[P_{j,i}] =3/8= E[n_i]. \qquad (10)$$

III. PROPOSED PEB

Based on (9) and (10), the PEB formula is derived. Then, the proposed PEB circuit is implemented by systematic steps that provide a simple and extendable solution for long fixed-width ($L \geq 16$) Booth multipliers.

A. Proposed PEB Formula

To easily understand the deduction process, we divide TPminor into two groups, i.e., TP*m*1 and TP*m*2, as displayed

in Fig. 1(b). Group TP*m*1 includes the columns containing n_i and can be derived as follows:

$$TPm1 = \frac{1}{4}(P_{L-2,0} + \ldots\ldots + P_{0,Q-1} + n_{Q-1}) + \frac{1}{16}(P_{L-4,0} + \ldots\ldots + P_{0,Q-2} + n_{Q-2}) + \ldots\ldots + 2^{-2Q}(P_{0,0} + n_0) \quad (11)$$

where $Q = L/2$. Substituting (7) and (8) into (11), the expected value of TPm1 can be simplified as

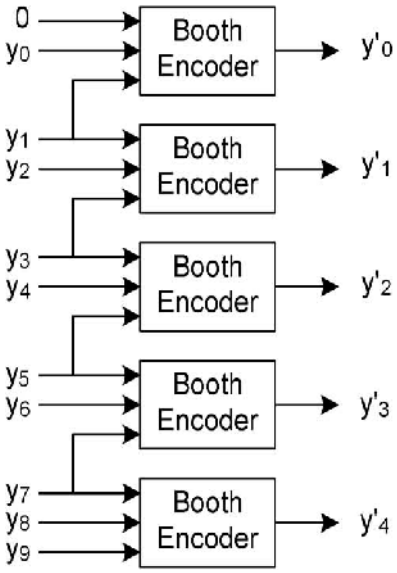


Fig. 1. Example of 10 × 10 Booth multiplier. (a) Booth encoder.

$$E[TP_{m1}] = \frac{3}{8}\sum_{i=1}^{Q-1}[(Q + 2 - i).2^{-2i}] + 2^{-2Q}. \quad (12)$$

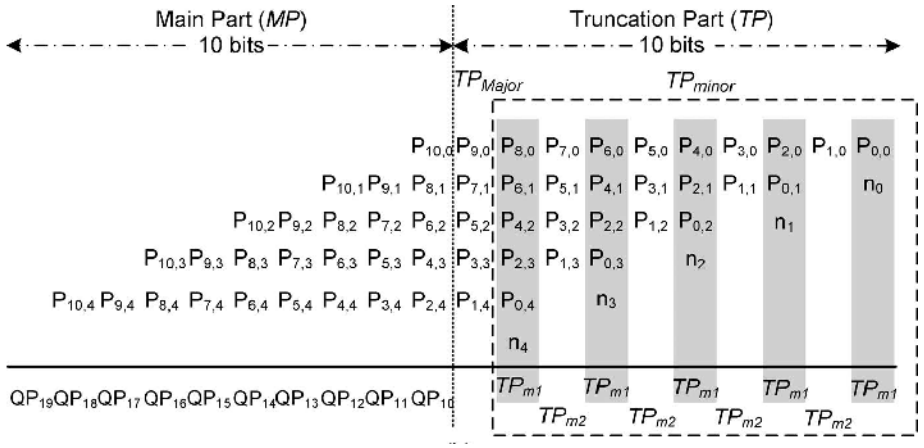


Fig. 1. Example of 10 × 10 Booth multiplier (b) Partial product array: MP and TP.

Similarly, the remaining group TP$m2$ and its expected value can be derived as follows:

$$\mathrm{TP}m2 = \frac{1}{8}(PL-3,0 + \ldots. + P1, Q-2) + \frac{1}{32}(PL-5,0 + \ldots + P1,Q-3) + \ldots\ldots + 2-2Q+1P1,0$$

$$E[\mathrm{TP}_{m2}] = \frac{3}{8}\sum_{i=1}^{Q-1}[(Q - i) \cdot 2^{-2i-1}] \qquad (13)$$

TABLE III:IMPLEMENTATION INDICES *A* AND *B* ACCORDING TO (15)

Combining (12) and (13), the expected value of TPminor can be calculated as follows:

$$E[\mathrm{TPminor}] = E[\mathrm{TP}m1] + E[\mathrm{TP}m2]$$

$$= \frac{3}{8}\sum_{i=1}^{Q-1}[(\frac{3}{2}Q + 2 - \frac{3}{2}i) \cdot 2^{-2i}] + 2^{-2Q}$$

$$= \frac{3Q}{16} + 2-2(Q+1) = \frac{3L}{32} + 2-2(L2+1) \qquad (14)$$

where the last term $2-2((L/2)+1)$ can be neglected because its value is smaller than the former term $3L/32$, particularly for large L. As a result, the expected value of TPminor can be estimated as follows:

$$E[\mathrm{TP}_{\mathrm{minor}}] \approx \mathrm{Round}(\frac{3L}{32})$$

$$= \mathrm{Round}(A.b)$$

$$= A + \mathrm{Round}(B/2) \qquad (15)$$

where A and b are the integer and fractional parts of $3L/32$, respectively. B is set to 1 if $b \geq 0.5$, otherwise $B = 0$.

Table III tabulates the values of A and B by (15) in various widths. Substituting (15) into (4), we obtain the PEB formula as follows:

$$\sigma = \text{Round}\left(\frac{1}{2}\,\text{TP}_{\text{Major}} + \frac{3L}{32}\right)$$
$$= \text{Round}\left(\frac{1}{2}\,(\text{TP}_{\text{Major}} + B)\right) + A \quad . (16)$$

B. Proposed PEB Circuit Using the Systematic Procedure

The realization of (16) can be easily implemented by using full adders (FAs) and half-adders (HAs). The PEB circuit is obtained after the following systematic steps:
1) Find integer *A* and bit *B* by calculating PEB in (15).
2) Generate *A* estimation carries ($ec_0 - ec_{A-1}$), and add them to the LSC of MP.
3) Sum up bit *B* and elements in set {TPMajor} = {PL−1,0, PL−3,1, . . . , P1,Q−1} with the FA or HA tree to produce the remaining estimation carries (ec*is*) being added to the LSC of MP and a sum (for rounding). The detailed procedure is listed as follows:

a) Add bit *B* and set {TPMajor} in the carry-save form [16] with sums to be repeatedly added for producing ec_{is} until only one sum is left.

b) Set the final sum as the last ec_i.Taking width $L = 10$ as an example, the proposed PEB circuit (gray block as shown in Fig. 2) can be obtained after conducting the proposed systematic steps. First, $A = 0$ and $B = 1$ are obtained from Table III. Second, no carry is generated because $A = 0$. Third, sum up B (= 1) and all elements of set {TPMajor} = {P9,0, P7,1, P5,2, P3,3, P1,4} with two FAs and one HA. The 10-bit Booth multiplier with the proposed PEB circuit is shown in Fig. 2. The systematic steps can be applied to the long fixed-width multiplication. For example, Fig. 3 displays the PEB circuit for the 32-bit fixed-width multiplication (A =3 & B = 0).

IV. PERFORMANCE COMPARISONS

A. Fixed-Width Booth Multiplier

In Table IV, Cadence System-on-Chip (SoC) Encounter is applied with Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm standard cell library to implement all the listed circuits, and the area (in square micrometers) and power consumption (in milli watts) comparisons are normalized to those of the post truncated Booth multipliers as shown in parentheses, respectively. The accuracy can be evaluated in terms of the absolute average error |€'|, the maximum error *€M*,

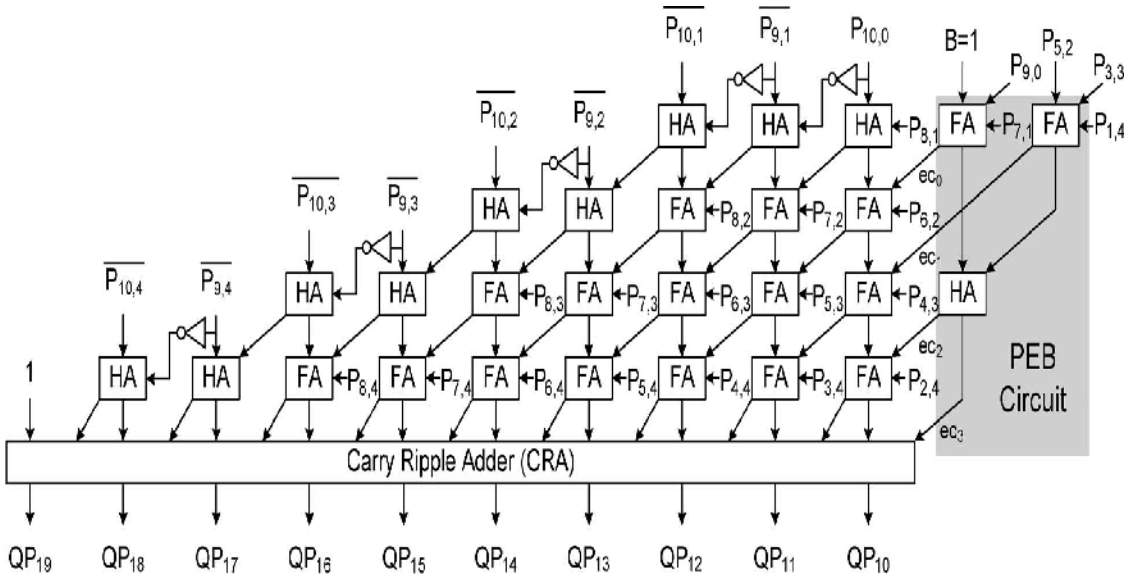


Fig. 2. Fixed-width 10-bit multiplier with the proposed PEB circuit.

TABLE IV
AREA AND POWER-CONSUMPTION COMPARISONS

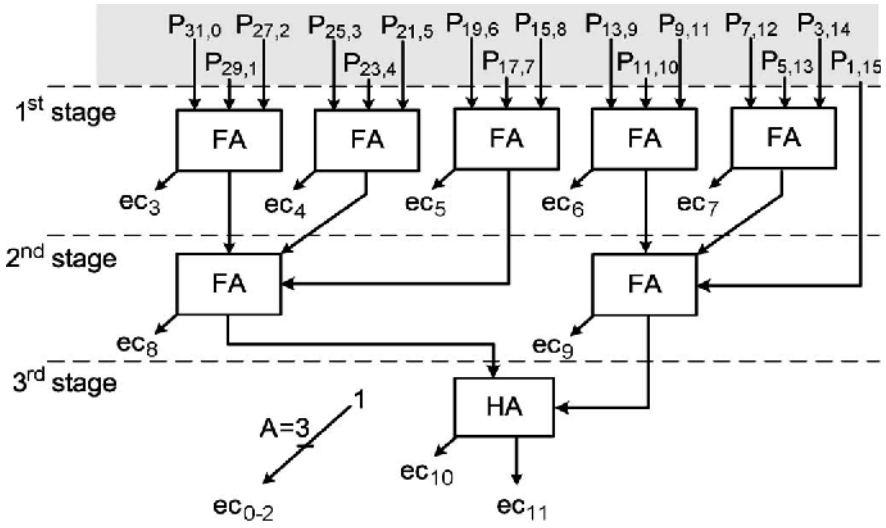
works	$L = 8$ Area / Power	$L = 10$ Area / Power	$L = 12$ Area / Power	$L = 16$ Area / Power
P.T.	100% / 100% (6770 / 1.597)	100% / 100% (10382 / 2.682)	100% / 100% (14774 / 4.106)	100% / 100% (25773 / 7.983)
[10]	65% / 61%	62% / 58%	60% / 57%	58% / 54%
[15]	64% / 60%	62% / 57%	60% / 55%	58% / 53%
[9]	57% / 54%	56% / 53%	55% / 52%	54% / 51%
[14]	57% / 53%	57% / 52%	55% / 51%	55% / 50%
PEB	58% / 55%	57% / 53%	56% / 53%	55% / 51%

mean square error €ms, the average error €', and the variance of absolute error €*v* defined as

$$|€'| = \text{Avg}\{|SP - QP|\} \quad €M = \text{Max}\{|SP - QP|\}$$

$$€ms = \text{Avg}|SP - QP|2\} \qquad €' = \text{Avg}\{SP - QP\}$$

$$€v = \text{Var}\{|SP - QP|\} \quad (17)$$



Where Avg{ · }, |N|, Max{ · }, and Var{ · } represent the average operation, the absolute value *N*, the maximum operation, and the variance operation, respectively. Table V shows the error comparisons of existing fixed-width Booth multipliers in various lengths *L*, where numbers in parentheses stand for the truncation errors of direct-truncated (DT) multipliers, which is defined in (17). Compared with that of [9] and [14], our proposed PEB circuit provides the smallest truncation errors

TABLE V

absolute average error |€'|, maximum error €*m*, mean square error €ms, average error €', and the variance of absolute error €*v* comparisons

L	works	$\lvert\bar{\epsilon}\rvert$	ϵ_M	ϵ_{mse}	$\bar{\epsilon}$	ϵ_v
8	D.T.	100% (384)	100% (1024)	100% (176158)	100% (384)	100% (28510)
	[10]	22.0%	37.5%	6.19%	8.85%	13.19%
	[15]	20.1%	29.2%	5.09%	0.52%	10.42%
	[9]	27.8%	43.3%	10.1%	0.1%	22.2%
	[14]	26.8%	43.3%	9.31%	1.38%	20.2%
	PEB	23.1%	37.5%	6.81%	0.00%	14.42%
	P.T.	16.6%	12.5%	3.10%	-0.52%	4.90%
10	D.T.	100% (1920)	100% (5120)	100% (4.3×10^6)	100% (1920)	100% (5.7×10^5)
	[10]	18.3%	30.0%	4.41%	6.46%	11.40%
	[15]	17.0%	30.0%	3.80%	-0.21%	9.64%
	[9]	24.8%	42.6%	8.30%	0.00%	22.2%
	[14]	24.5%	42.6%	8.01%	0.41%	21.16%
	PEB	21.2%	40.0%	6.00%	10.0%	15.95%
	P.T.	13.3%	10.0%	2.05%	-0.13%	3.88%
12	D.T.	100% (9216)	100% (24576)	100% (9.6×10^7)	100% (9216)	100% (1.1×10^7)
	[10]	15.9%	33.3%	3.42%	5.64%	10.51%
	[15]	14.8%	27.8%	2.93%	0.09%	8.84%
	[9]	22.6%	42.2%	7.00%	0.0%	22.2%
	[14]	22.5%	42.2%	6.94%	0.13%	21.74%
	PEB	17.9%	33.3%	4.37%	-5.55%	13.39%
	P.T.	11.1%	8.33%	1.46%	-0.03%	3.24%
16	D.T.	100% (196608)	100% (524288)	100% (4.2×10^{10})	100% (196608)	100% (3.7×10^9)
	[10]	12.7%	31.3%	2.27%	4.18%	9.20%
	[15]	11.9%	27.1%	1.99%	0.02%	7.99%
	[9]	19.5%	41.6%	5.40%	0.00%	22.33%
	[14]	19.5%	41.6%	5.39%	0.01%	22.23%
	PEB	15.9%	31.3%	3.54%	-8.33%	14.18%
	P.T.	8.33%	6.25%	0.85%	0.00%	2.44%

except the average error with the same or 1% more hardware overhead. It is also interesting to observe that the designs of [10] and [15] outperform [9], [14], and our proposed PEB circuit in these error merits using more hardware. In general, a tradeoff exists between hardware overhead and accuracy in these compensation circuits. The larger hardware overheads of [10] and [15] come from the bias generation circuits and encoders. Because our compensation bias is derived from a theoretical deduction, our PEB circuit could be easily extended

TABLE VI

ACCURACY AND AREA COMPARISONS

	PSNR	AREA μm² (%)
Standard	56.1	223428(100%)
DT	34.62	166919(75%)
PEB	52.04	171825(77%)

Characteristics	
Technology	0.18 μm
Power Supply	1.8V
Core Size	501 μm × 508 μm
Gate Count	17.2K
Max. Freq.	55MHz
Power	12.4mW@55MHz

Fig. 4. Core layout and characteristics of the DCT core using the proposed PEB circuit.

for high-accuracy fixed-width multiplication using more information from TPminor with the penalty of more area. Different from previous compensation circuits for Booth multipliers, our PEB circuit does not need the exhaustive simulation and the heuristic bias circuit design.

B. Application Example: DCT

In order to exhibit the accuracy in real applications, the proposed low-error PEB is applied into an 8×8 2-DDCT [17]. The size of the test image "Lena" is 512×512 pixels, with each pixel being represented by 8-bit 256-gray-level data. Moreover, the accuracy performance of the DCT core is evaluated by the peak signal-to-noise ratio (PSNR). The comparison results for the accuracy of the PSNR and the synthesized area are tabulated in Table VI. Compared with the DCT core using standard Booth multipliers, the DCT core using the proposed PEB circuit reduces 23% area with the PSNR penalty of 4 dB. On the other hand, the accuracy the PSNR of the DCT core using the proposed PEB circuit is more than 17 dB, which is larger than the DT approach with only 2%more hardware overhead. To implement the DCT with the proposed PEB circuit on a chip, we use the Synopsys Design Compiler to synthesize the register-transfer-level design and Cadence SoC Encounter to run placement and routing. Fig. 4 shows the layout view and the characteristics of the architecture. While implemented in a 1.8-V TSMC 0.18-μm 1P6M CMOS process, the proposed DCT core can be operated in a 55 MHz clock rate, and the core size is 501μm×508μm.

V. CONCLUSION

In this brief, we have first derived the PEB formula and have applied the probabilistic analysis for the truncated two's complement fixed-width Booth multiplier. Then, a simple and systematic procedure has been presented to design the compensation circuit based on the PEB formula and the probabilistic analysis. Compared with the existing works, the proposed method has provided smaller area and smaller truncation errors. The realization of our PEB circuit does not need exhaustive simulations and heuristic compensation strategies that tend to introduce curve fitting errors and unacceptable exponential simulation time. Furthermore, the proposed PEB Booth multiplier in the DCT application has shown the improvement of the PSNR by 17 dB with only 2% area penalty compared with the DT method. In the future work, our PEB circuit can be applied for high-accuracy fixed-width multiplication using more inputs from TPminor with more hardware overhead.

REFERENCES

[1] J. P. Wang, S. R. Kuang, and S. C. Liang, "High-accuracy fixedwidth modified Booth multipliers for lossy applications," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 1, pp. 52–60, Jan. 2011.

[2] M. J. Schulte and E. E. Swartzlander, Jr., "Truncated multiplication with correction constant," in VLSI Symp. Tech. Dig., 1993, pp. 388–396.

[3] S. S. Kidambi, F. El-Guibaly, and A. Antoniou, "Area-efficient multipliers for digital signal processing applications," IEEE Trans. Circuits Syst. II,
Analog Digit. Signal Process, vol. 43, no. 2, pp. 90–95, Feb. 1996.

[4] J. M. Jou, S. R. Kuang, and R. D. Chen, "Design of lower-error fixedwidth multipliers for DSP applications," IEEE Trans. Circuits Syst. II,
Analog Digit. Signal Process, vol. 46, no. 6, pp. 836–842, Jun. 1999.

[5] L. D. Van, S. S. Wang, and W. S. Feng, "Design of the lower-error fixedwidth multiplier and its application," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, vol. 47, no. 10, pp. 1112–1118, Oct. 2000.

[6] L. D. Van and C. C. Yang, "Generalized low-error area-efficient fixedwidth multipliers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52,
no. 8, pp. 1608–1619, Aug. 2005.

[7] Y. C. Liao, H. C. Chang, and C. W. Liu, "Carry estimation for two's complement fixed-width multipliers," in Proc. IEEE Workshop on Signal
Process. Syst. Design Implementation, 2006, pp. 345–350.

[8] N. Petra, D. D. Caro, V. Garofalo, E. Napoli, and A. G. M. Strollo, "Truncated binary multipliers with variable correction and minimum mean
square error," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 6, pp. 1312–1325, Jun. 2010.

[9] S. J. Jou, M. H. Tsai, and Y. L. Tsao, "Low-error reduced-width Booth multipliers for DSP applications," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 50, no. 11, pp. 1470–1474, Nov. 2003.

[10] K. J. Cho, K. C. Lee, J. G. Chung, and K. K. Parhi, "Design of low-error fixed-width modified Booth multiplier," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 522–531, May 2004.

[11] T. B. Juang and S. F. Hsiao, "Low-error carry-free fixed-width multipliers with low-cost compensation circuits," IEEE Trans. Circuits Syst. II, Exp.Briefs, vol. 52, no. 6, pp. 299–303, Jun. 2005.

[12] K. K. Parhi, J. G. Chung, K. C. Lee, and K. J. Cho, "Low-error fixed-width modified Booth multiplier," U.S. Patent 7 334 200, Feb. 19, 2008.

[13] H. A. Huang, Y. C. Liao, and H. C. Chang, "A self-compensation fixedwidth Booth multiplier and its 128-point FFT applications," in Proc. IEEE ISCAS, 2006, pp. 3538–3541.

[14] M. A. Song, L. D. Van, and S. Y. Kuo, "Adaptive low-error fixed-width Booth multipliers," IEICE Trans. Fundam., vol. E90-A, no. 6, pp. 1180– 1187, Jun. 2007.

[15] Y. C. Lim, "Single-precision multiplier with reduced circuit complexity for signal processing applications," IEEE Trans. Comput., vol. 41, no. 10, pp. 1333–1336, Oct. 1992

[16] B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs.. Oxford, U.K.: Oxford Univ. Press, 2000.

[17] S. C. Hsia and S. H. Wang, "Shift-register-based data transposition for cost-effective discrete cosine transform," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 6, pp. 725–728, Jun. 2007.