Mote Design Supported with Remote Hardware Modifications Capability for Wireless Sensor Network applications

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ABSTRACT

Many Wireless Sensor Networks (WSNs) applications are new and their requirements may not be fully anticipated during the sensor networks design and development stage. We are presenting a sensor network infrastructure that support motes' with remote hardware and software modification to match the target applications need. Using the proposed infrastructure in next-generation WSNs will produce flexible infrastructures that will provide over-the-air remote design modification even after the deployment of WSNs on the sensing field.

In this paper, we are presenting the design concept and challenges of such infrastructure. Also, we present the use of the infrastructure in one possible environmental monitoring application such as forest fire. The development of such infrastructure will have an impact on advances the research on the real-time remote sensing, heterogeneous WSN, and WSNs applications.

KEY WORDS:

WSN, Mote design, FPGA

1. INTRODUCTION

Recent advances in wireless communications and electronics have enabled the development of wireless sensor networks that use low-cost, low-power, multifunctional sensor motes. These tiny motes design consist of integrated sensing, computing, communication units, and some other application-dependent units such as power generators and location finding units [1-3]. Such networks offer economically viable solutions for applications that can be found in different settings such as industry, military, environment, health, etc. [4, 5]. Sensor motes are generally designed and programmed to match the needs of the target applications before they are released to the field. We present WSN mote design that can provide remote software reprogramming and hardware modification capabilities, which called throughout this paper as "RH-mote". This type of mote is not available in existing WSN infrastructure. Therefore, it is crucial to explore the design and the use of such motes in next-generation WSNs, which require on-field system modifications. The design and the development of the proposed RH-mote will provide WSNs with dynamically adaptable feature. Such feature will provide motes with design adjusting capability to the surrounding environment even after the deployment of the RH-mote on the sensing field.

Supporting the proposed RH-mote infrastructure with hardware modifications capability will require the use of FPGA technology in motes design. The existing WSNs motes are not usually supported with FPGA in their designs due to the main drawback of the FPGA, which is high power consumption. However, such drawback can be resolved with the use of modern FPGA chips that consume low power, and the use of partial reconfigurations technique exists in some FPGA design tools such as Xilinx PlanAhead. Partial reconfiguration can reduce the size of the design file, also called design bit file, which will support fast remote hardware modification with less power consumption.

Despite the use of low power FPGA technology and partial reconfiguration technique, the use of FPGA in motes design will still consume more power than those motes designed using microcontrollers. Therefore, a low-cost tiny solar unit has been used in this project to recharge the RH-mote's batteries. This will provide long operation time and elevate the drawback for the large power consumption of using FPGA in the proposed infrastructure. The increase in motes' cost due to the use of solar units in next-generation motes will not be acceptable for low-cost WSNs. Nevertheless, the motes increasing cost is acceptable where they are deployed in some applications that have well-setting environments, i.e., careful consideration to motes distributions on applications that are exposed to daylight, which will help recharge motes' batteries. Environmental monitoring applications such as forest fire monitoring can be considered as one of the well-setting applications that can use the RH-mote infrastructure.

2. RH-MOTE'S DESIGN CONCEPT AND CHALLENGES

Sensor motes in some existing WSNs have the support for software reprogramming capability. For example, the SOS project at UCLA provides software modifying on individual motes of a sensor network after the network has been deployed and initialized. The incremental update ability for new software modules and removed unused software module after network deployment have been implemented in SOS project [6]. Also, the lightweight virtual machines such as Mate and modular operating systems such as Contiki are using incremental code updates. Therefore, in this RH-mote infrastructure project, the focus will be given to the hardware modifications capability since it is a new feature for WSNs that has not been investigated thoroughly yet [7].

The main design challenges of supporting RH-mote infrastructure development with remote hardware modifications are as follows:

i) **Minimizing RH-mote's power consumption**: One of the main characteristics of the WSNs is the use of low power motes. Typically, the mote should able to work for a year using an AA battery. However, the RH-mote infrastructure design has to use FPGA technology to provide remote hardware modifications, which is generally a power hungry technology. RH-mote infrastructure's power consumption can be reduced by using some of the recently developed FPGA chips that consume low power. This may include Actel Igloo, and Xilinx Spartan 6. In addition, using partial reconfiguration technique supported by some FPGA design tools such as Xilinx PlanAhead, could reduce the size of the FPGA design file required for remote hardware modification, which significantly reduces power consumption. It is known that the power consumption of transferring one bit is equal to the execution of 1000 instructions [8].

To elevate the FPGA high power consumption problem, the use of a large battery unit may support mote operation for extended period of time. However, the battery charge will eventually be depleted when a mote serves the target application for long period of time. We believe that using a solar-based charging battery unit for the mote design will be very suitable for well-setting

environment monitoring application. As the solar charging battery units are small in size and inexpensive, it is feasible and acceptable for using these units for recharging the RH-mote infrastructure. This provides long battery life even when the FPGA is used in mote design.

ii) **Wireless JTAG:** The JTAG port supported with FPGA chips is commonly used for their hardware modifications. Typically, the design is downloaded from a computer to FPGA chip using the JTAG port. To modify the design of the motes that use the proposed infrastructure located on the application field, a wireless JTAG unit needs to be used to receive the design file and deliver it to the JTAG port of the FPGA chip on the RH-motes. However, since the wireless JTAG unit is currently not available as a commercial product; therefore, such unit will need to be designed and developed for the proposed RH-mote infrastructure.

iii) **Design and development of a reconfigurable components library**: The RH-mote infrastructure is intended to have a flexible design to support the need of the target applications that have different requirements. Therefore, a library that includes flexible and reconfigurable components is required to be designed to fulfill the applications' needs. The design of the library to include the components that required to supports different applications will be a large task. Therefore, the library design will target only the components development for RH-mote infrastructure that required supporting forest fire monitoring application. For example, a set of components for the sensors interfaces such as CMOS pixels, temperature, and humidity sensors - in addition to the soft-core MIPS processor component, wireless transceiver interface, and JTAG controller - will be included in the components library's developments. These components will be developed using VHDL language and synthesized using the FPGA design tools.

3. RH-MOTE INFRASTRUCTURE DEVELOPMENT

The strategy for the RH-mote infrastructure development is based on integrating all RH-mote's components on on FPGA chip. The mote's FPGA chip includes the soft components required for the mote design such as processor, sensor interfaces, JTAG controller, memory and wireless transceiver interfaces and controllers. In addition to these soft components, other

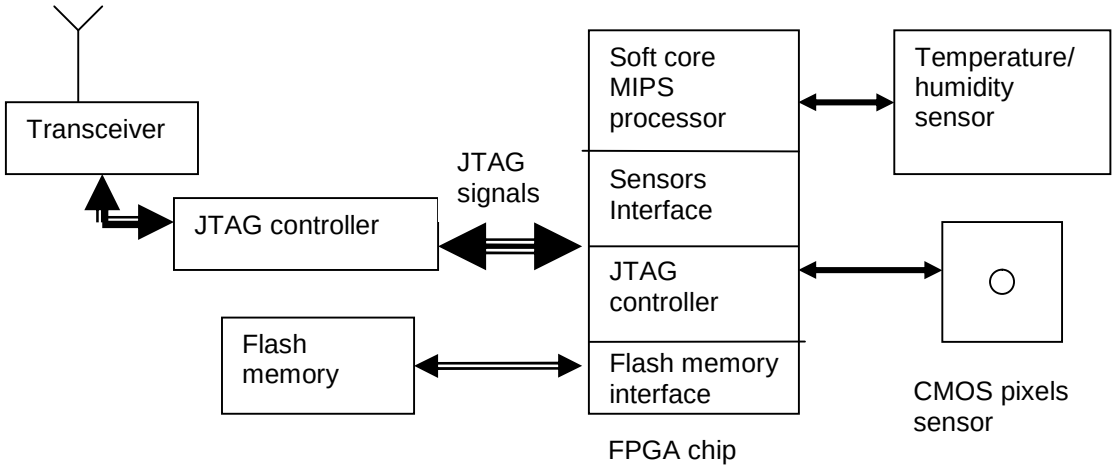

Figure 1 RH-mote infrastructure architecture

off-the-shelf components such as the temperature/humidity sensor, CMOS pixels sensor, memory, wireless transceiver, solar unit, and mote's batteries have been integrated with the soft components and placed on the RH-mote's PCB board [Figure 1]. The VHDL language has been used to design all soft cores used in the mote design such as processor and sensors interfaces.
The main components of the RH-mote are as follow:

3.1. Soft core MIPS processor

Currently available WSNs motes support basic sensing capability and use standard processing elements. The ATmega128 micro-controller can be considered the most commonly used processing element for sensing motes. However, the ATmega128 uses an 8-bit architecture and is thus not as efficient as 16 and 32-bit based architectures in achieving intensive processing that required in some next-generation WSNs applications. Generally, the processing cores used on existing WSNs motes are off-the-shelf custom made VLSI processors that provide reprogramming capability and have no hardware modification capability.

A soft core processor architecture has been designed for RH-mote, which is optimized, flexible, and efficient for the need of the WSN application. The instructions set and the architecture of the soft core processor has been optimized to the needs of the target WSN

application. In addition, the soft core design approach for the RH-mote processor has a flexible design that can support remote hardware modification on the applications field. We have used MIPS architecture for the soft core processor since the basic non-pipeline MIPS core has simple and efficient architecture. Also, the processing core is small and can be integrated on the low-power FPGA chip.

The PI and his research team have developed specialized 32-bit non-pipelined MIPS soft-core processor for senor network motes [Figure 2]. The developed soft-core processor has 10MIPS performance, which is acceptable for some sensor

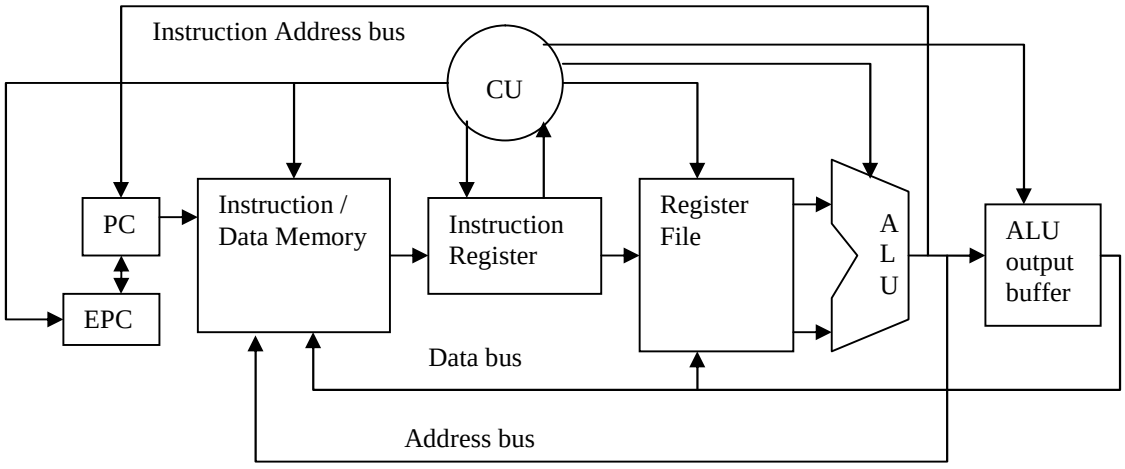

Figure 2: Soft Core Processor Architecture for RH-mote

networks motes applications [9]. Developing MIPS pipelined core can be used for next-generation sensor networks motes to support higher processing performance, remote design modifications, and heterogeneous WSNs.

3.2 Wireless JTAG unit

Most FPGA chips use a JTAG port to download the design file to target FPGA chip. As the RH-motes will support remote hardware modifications capability on the application field and therefore, a wireless JTAG unit has to be design with each WSN's mote. Developing a wireless JTAG port is essential for this project since no commercially available FPGA chip that has wireless JTAG. The development strategy for the JTAG unit is to use fast wireless transceiver and CPLD-based controller to generate the signals and timing for the JTAG port.

The design bit file size produced by the Xilinx design tools has a default size of 344,468 bytes. However, using the file compression option of the Xilinx design tools, the design bit file size can be reduced significantly. We have evaluated the transfer time for the ALU design bit to modify the soft core processor that designed using Spartan device XA3S200A and we found it required 6.1 seconds to download ALU design to FPGA chip.

Clearly, the transfer time for the hardware modification components was large due to the use of slow transceiver of 56Kbit/sec. Using faster transceiver will help to speed the RH-mote design modifications. The transmission range for the transceiver used in the preliminary study was 100-feet.

This transmission range is acceptable for some applications and used in the developed WSN prototype for environment monitoring where all RH-motes will be placed in distance of 100-feet or less from each other. The design bit file for the ALU component is segmented into packets and transferred using the data packet frame format that developed by our research group, which has 8-bit header and 8-bit trailer, 8-byte size for the hardware modification file transfer, and a CRC field.
Each RH-mote infrastructure will use a CPLD chip to control the received data from the wireless channel and deliver it to the JTAG port on the FPGA located on the RH-mote board to perform hardware modification.

3.3. Sensor interfaces

There are many off-the-shelf sensors available today. However, only those sensors required to serve the target application will be placed on the PCB board of the proposed RH-motes. Off-the-shelf sensors, such as CMOS pixels and temperature/humidity, will be utilized by the RH-mote to serve the forest fire monitoring application and to provide a proof-of-concept for using remote hardware modification capability.

The RH-mote infrastructure, the VHDL soft core has developed for the CMOS pixels sensor. Also, the soft core for the LCD interface was developed since LCD will be useful for the target application and specifically for the base station design. The RH-mode supported with a VHDL processing unit that can capture and analyze the image on the sensor mote. In addition, a VHDL based display unit was designed to control small LCD display unit, which is a useful component for monitoring applications and specifically on the base station of the WSN.

The development strategy for the interfaces design research is to place the pixels sensor on the PCB board of the RH-mote infrastructure, which will include the FPGA chip and memory to save the captured image and analyze it by the algorithm processed on the FPGA chip.

3.4. Recharging the battery unit

Despite the use of low power FPGA chip and partial reconfiguration technique in the design of the RH-mote to reduce the power consumption, we plan to use a solar unit for recharging the RH-mode's battery. Using a solar unit in a well-setting environment will provide the RH-mote with a sustain power. A tiny and low-cost off-the-shelf battery recharging solar unit is available such as the one that can charge one AA battery and cost less than $10 for a unit [Figure 3]. Clearly, the cost of the proposed mote will be increased due to the use of the solar recharging unit. However, such cost will be acceptable for the use in WSNs serving environmental monitoring applications.

4. WSN PROTOTYPE DEVELOPMENTS

We are developing a WSN prototype to provide a proof-of-concept for using remote hardware modification and software reprogramming capability of the RH-mote infrastructure in WSN applications. A small size WSN prototype that has few clusters of 10 motes each will be developed [Figure 4].

A forest fire monitoring application will be used to demonstrate the use of RH-motes, which can be modified remotely their soft processing cores on the application field. Each RH-mote has three sensors: humidity, temperature, and CMOS pixels. The remote hardware modifications capability of the proposed mote will be used to remotely modify the processing core of each mote to match the needs of the surrounding application environment. There are different possible scenarios of using the RH-motes on forest fire monitoring. However, we will use one possible scenario that

Figure 3 Tiny solar battery recharging unit

will explore the dynamic modification of motes' soft-core processors to support different processing capabilities in each RH-mote that deployed on the application field. Each RH-mote at the WSN developed prototype will check the humidity level at surrounding environment. When the humidity drops to a low level, this is either an indication of dry weather or a start of a fire around the mote's location. The mote at that area will then switch to check the temperature and when the temperature level is reached above a certain level, the mote will switch to scan the captured image of the surrounding forest to verify occurrence of fire. While the mote located at the fire area will locally process the captured images to identify the existence of fire, other motes located distantly from the fire will need to process the basic and simple operation of checking

humidity or temperature. The processing required for capturing and analyzing the fire image is more complex than the processing required for analyzing the sensors reading of humidity or temperature. Therefore, all ALU instructions and soft processor capabilities will be used by mote(s) located near the fire location while other motes will use fewer ALU instructions and small soft processor core capabilities for humidity and temperature sensing. Clearly, heterogeneous processing cores will be dynamically implemented on WSN motes. Simple soft processing core will be used by all motes on WSNs at the start of the WSN and under normal operation mode, i.e., no fire is detected. As high temperature is detected near an RH-mote, the operation mode of the sensing mote will activate the image analyzing process, which requires the use of all soft core processing resources. However, when fire is not detected, the mote's processing core will be restored to its temperature sensing mode.

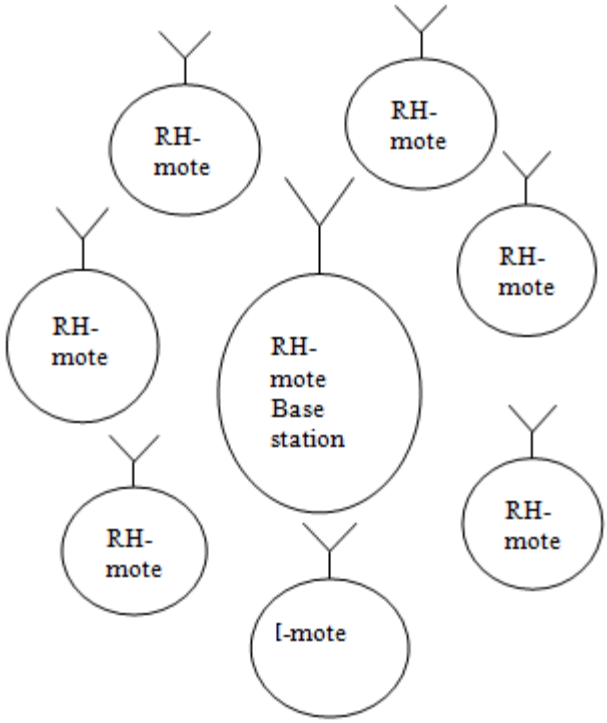

Figure 4 One WSN cluster use RH-motes

As all motes use basic soft processing at the start and under normal WSN operations, implementing hardware modification capability in WSN will help to save a lot of power. This power can be utilized on having a soft processor with full resources and capabilities that can be used with all motes during the starting operation mode of the WSN. The deployment of soft processors in all motes that are capable to detect forest fire will consume unnecessary power for detecting fire, which might occur from time to time. Moreover, the forest fire image will be captured and sent to the base station for image verification by the WSN operator, which will appear on the LCD display on the base station.

5. CONCLUSION

We presented the concept and the challenges in designing RH-mote that can support remote hardware and software modifications. The development of such mote infrastructure will have an impact on advances the research on the real-time remote sensing, heterogeneous WSN, and WSNs applications. The RH-mote's infrastructure can be used in Environmental monitoring such as forest fire applications. Using FPGA chips in RH-motes will consume large power. However, we propose using a low-cost tiny solar unit to recharge the RH-mote's batteries. This will provide long operation time and elevate the drawback for the large power consumption of using FPGA in the proposed infrastructure.

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