DESIGN OF A LINEAR AND WIDE RANGE CURRENT STARVED VOLTAGE CONTROLLED OSCILLATOR FOR PLL

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ABSTRACT

This paper focuses on design and analysis of Current Starved Ring Voltage Controlled Oscillators (CSVCO) for PLL application. The CSVCO circuit is designed and simulated using GPDK 180nm CMOS Technology. The CSVCO has frequency range from 53 MHz to 2.348 GHz and power consumption is 848µW. The jitter is improved by connecting a D Flip Flop. In this design the maximum time jitter after D flip flop is 3.1ps and 1.5ps for rising and falling edge respectively and output frequency is from 173MHz to 1.2GHz. The supply voltage V_{DD} is 1.8V.

KEYWORDS
Ring Oscillator, Voltage Controlled Oscillator (VCO), Current Starved Voltage Controlled Oscillator (CSVCO).

1. INTRODUCTION

In VLSI field the design of a linear and wide range voltage controlled oscillator for RF application is a challenging work for Electronics Engineers. VCO is the main component in the many RF circuits. VCO is the heart of Phase Lock Loop system. An oscillator is an autonomous system which generates a periodic output without any input. The VCO is an electronic circuit which produces the frequency signal depending on its input voltage. VCO is voltage to frequency converter. The Barkhausen criteria for oscillation can be met without resonators as in ring oscillators. If the open loop circuit exhibits sufficient gain at the zero phase frequency, oscillations occurs. The important requirements of VCO are Frequency accuracy, wide tuning range, tuning linearity, low power consumption, small size and low phase noise [1].

2. DIFFERENT ARCHITECTURES OF VCO

The different architectures of VCO are

2.1. LC VCO

These VCO's are made by using inductors and capacitors, with an amplifier. A very high frequency voltage controlled oscillations are generated by using inductors and capacitors. This architecture is preferred for sinusoidal wave output and can be integrated where space is not important issue.

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2.2. Source Coupled VCO

These VCOs are made by using transistors connected back to back. This technique gives high frequency VCOs. These are also used to generate rectangular and saw tooth wave forms. These VCOs can be designed to dissipate less power than the current-starved VCO. The major disadvantage of these configurations is the need for a capacitor, something that may not be available in a single-poly pure digital process without using parasitic.

2.3. Current Starved Ring VCO

These VCOs are made by using ring oscillator. The ring oscillator works by controlling the charging and discharging of the gate capacitance of the next inverter. Decreasing the peak available charging current increases the time to charge and discharge the gate capacitance; consequently, the frequency is decreased [7]. Ring oscillators generate high frequency up to 10 GHz.

3. TRANSFER FUNCTION OF VCO

Ideally the VCO must be capable of transfer the input voltage to frequency linearly as shown in Figure 1.

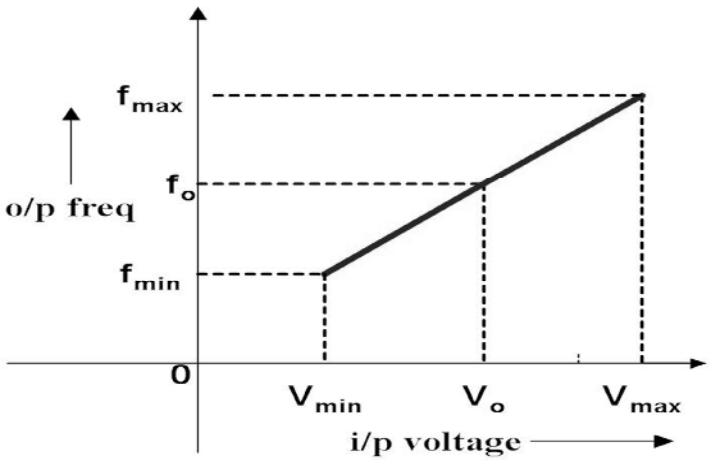

Figure 1. Transfer Function of VCO

The output frequency of the VCO is given by

$$\omega_{out} = \omega_0 + K_{VCO}.V_{invco} \text{ rad/sec} \quad (1)$$

where

V_{invco} is the input voltage to the VCO,

ω_o is the free running frequency,

K_{VCO} is the gain of the VCO and is given by

$$K_{VCO} = 2\pi.\frac{f_{max}-f_{min}}{V_{max}-V_{min}} \text{ rad/sec-volts} \quad (2)$$

4. VCO DESIGN

4.1. VCO Design parameters

The VCO designed according to the following specifications as shown in Table 1.

Table 1. VCO Design Specifications

Parameter	**Value**
Power supply (V_{DD})	1.8 V
Centre frequency	1GHz
No of inverter stages	3
Inverter delay	35ps
Random jitter (rms)	< 20ps
Technology	GPDK 180nm

4.2. Ring oscillator

The ring oscillator is made up of 3 inverters connected in ring fashion as shown in Figure 2. The length is fixed at 180nm. The width of PMOS transistor is 3 µm and width of NMOS is 700nm is considered for switching point (V_{SP}) at 0.9V. The average delay of each inverter with an inverter as load is 35ps.

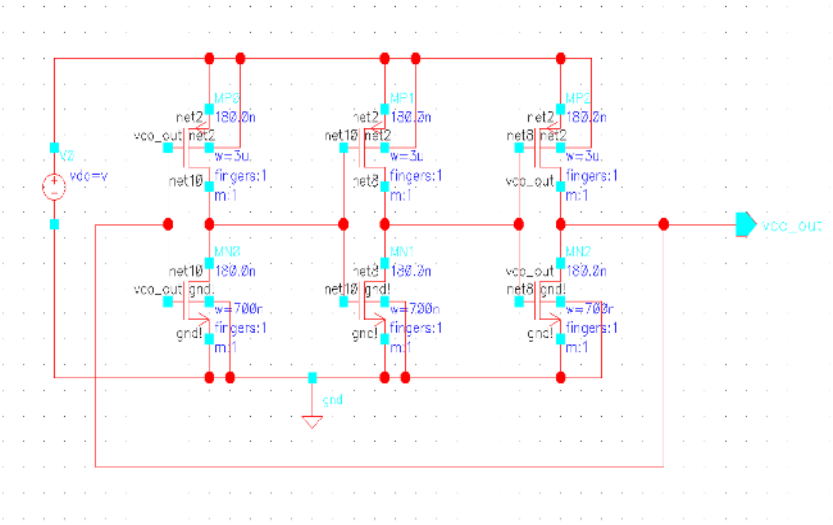

Figure 2. Schematic of Ring Oscillator.

The frequency of this ring oscillator will be

$$f_{osc} = \frac{1}{2.N.T_d} \text{ Hz} \tag{3}$$

where
N is number of inverter stages = 3
T_d is the average time delay of each inverter = 35ps
Oscillation frequency is 4.698GHz.

4.3. Why current starved architecture?

The V_{DD} varies ±10% of 1.8V i.e. from 1.62V to 1.98V. For this voltage variation the Ring architecture produces an output frequency from 4.175GHz to 5.077GHz with the difference of 992MHz, which is large variation as shown in Figure 3.

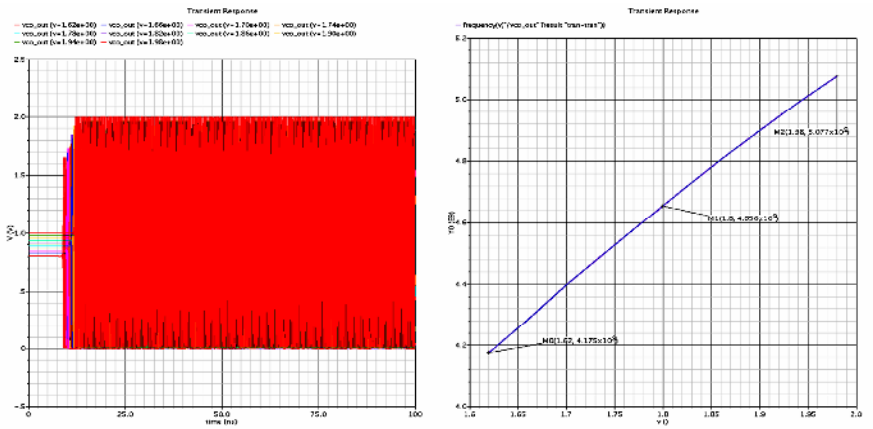

Figure 3. Vdd versus output frequency of ring VCO.

The output frequency is not stable when it is dependent on V_{DD}. This is made stable by supplying current to each inverter instead of V_{DD} as shown in Figure 4.

4.4. Current Starved VCO

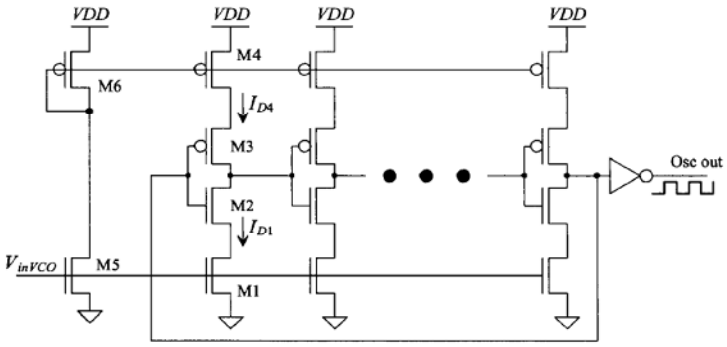

Figure 4. Schematic of Current Starved VCO [2]

The schematic of current-starved VCO is shown in Figure4. Its operation is similar to the ring oscillator. MOSFETs M2 and M3 operate as an inverter, while MOSFETs Ml and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the transistor M2 and M3. In other words, the inverter is starved for current. The drain currents of MOSFETs M5 and M6 are the same and are set by the input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage.

The total capacitance on the drains of M2 and M3 is given by

$$C_{tot} = C_{out} + C_{in} \tag{4}$$

$$C_{tot} = C'_{ox}(W_p L_p + W_n L_n) + \frac{3}{2} C'_{ox}(W_p L_p + W_n L_n) \tag{5}$$

This is simply the output and input capacitances of the inverter.This equation can be written in a more useful form as

$$C_{tot} = \frac{5}{2} C'_{ox}(W_p L_p + W_n L_n) \tag{6}$$

The time taken to charge C_{tot} from zero to V_{SP} with the constant current I_{D4} is given by

$$t_1 = C_{tot} \cdot \frac{V_{SP}}{I_{D4}} \tag{7}$$

where V_{SP} is switching point of the inverter.
While the time taken to discharge C_{tot} from V_{DD} to V_{SP} is given by

$$t_2 = C_{tot}.\frac{V_{DD}-V_{SP}}{I_{D1}} \quad (8)$$

If we set $I_{D4}= I_{D1}= I_D$ (which we will label $I_{Dcentre}$ when $V_{inVCO} = Vdd/2$), then the sum of t_1 and t_2 is simply

$$t_1 + t_2 = \frac{C_{tot}.V_{DD}}{I_D} \quad (9)$$

The oscillation frequency of the current-starved VCO for N (an odd number > 3) stages is

$$f_{osc} = \frac{1}{N(t_1+t_2)} = \frac{I_D}{N.C_{tot}.V_{DD}} \quad (10)$$

which is equal to f_{center} (at $V_{inVCO} = V_{DD}/2$ and $I_D = I_{Dcenter}$). The VCO stops oscillating, when $V_{inVCO} < V_{TN}$. Therefore, we can define $V_{min} = V_{TN}$ and $f_{min}= 0$. The maximum VCO oscillation frequency, f_{max} is determined by finding I_D when $V_{inVCO}=V_{DD}$. At the maximum frequency, $V_{max}= V_{DD}$.

4.5. Linearizing VCO Gain

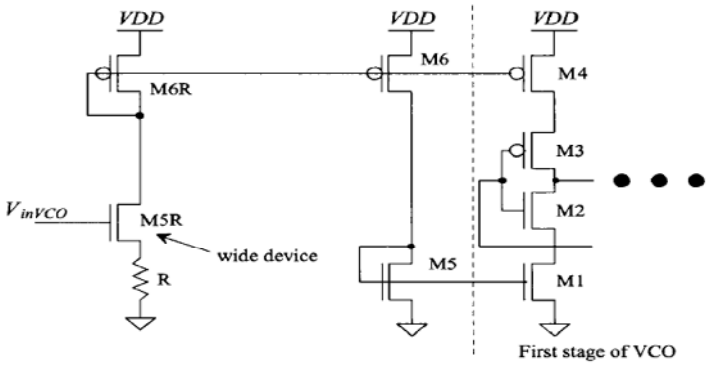

Figure 5. Linearizing VCO Gain [2]

To make the current in a MOSFET linearly related to the VCO's input voltage, consider the circuit shown in Figure 5. The width of M5R is made wide so that its V_{GS} is always approximately V_{TN}. Note that the current in M6R is mirrored over to M6 and M5 to control the current used in the current-starved VCO.

The drain current of M5R is shown in Figure 6. The drain current linearity is also depends on the width of M6R transistor. The width of M6R is 10µm and the width of M5R is made high and is taken as 100µm. The Figure 6 shows the V_{inVCO} vs drain current of M5R transistor. Drain current is linearly dependent on V_{inVCO}.

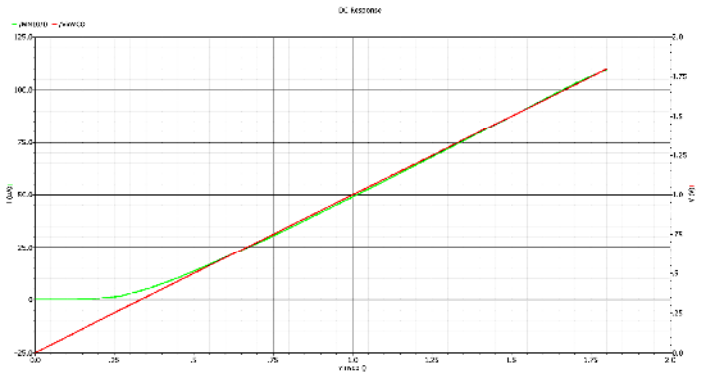

Figure 6. Drain current of M5R versus V_{inVCO}.

The average current drawn by the VCO is

$$I_{avg} = N.\frac{V_{DD}C_{tot}}{T} = N.V_{DD}.C_{tot}.f_{osc} \quad (11)$$

or $I_{avg} = I_D$ 12)

The average power dissipated by the VCO is

$$P_{avg} = V_{DD}.I_{avg} = V_{DD}.I_D \quad (13)$$

5. IMPLEMENTATION AND RESULTS

The final design of linear wide range current starved voltage controlled oscillator is shown in Figure 7.

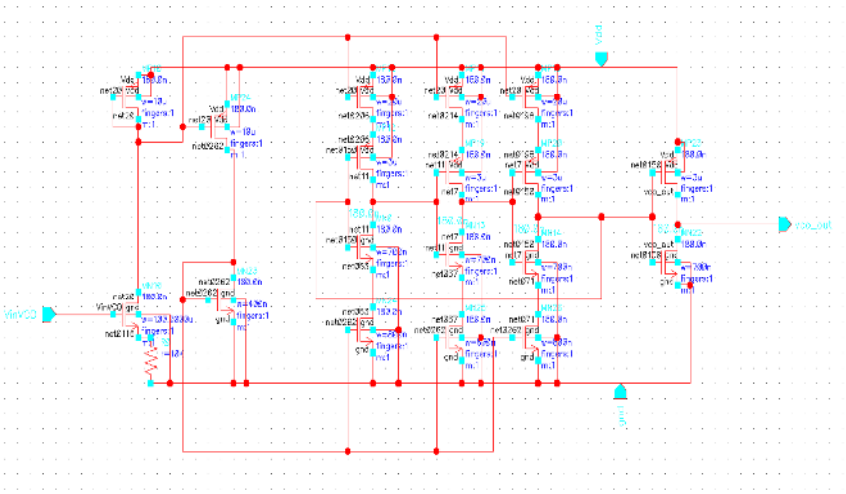

Figure 7. Complete Current Starved VCO

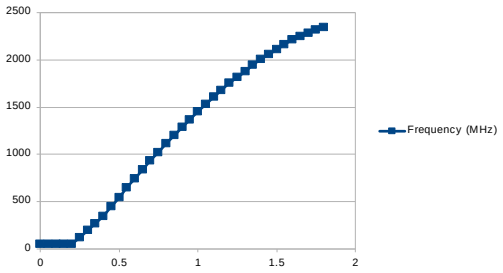

Figure 8. Vinvco versus output frequency

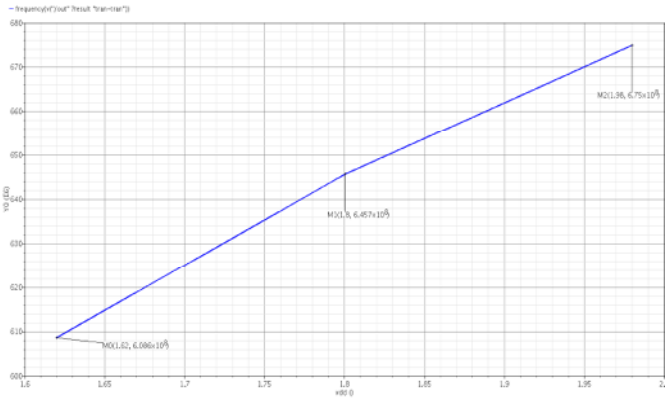

Figure 9. Vdd versus output frequency of current starved VCO in cadence, difference is 64MHz.

It is observed from Figure 9 that the variation in V_{DD} from 1.62V to 1.98V i.e. ±10% of 1.8V, which varies the output frequency by 64MHz. Therefore the output frequency of VCO is controlled by current. This produces stable oscillations irrespective of V_{DD} variations.

5.1. Jitter Improvement

The jitter of the complete current starved VCO is as shown in Figure 10. The Figure 11 shows the eye diagram of output waveforms of the VCO after divider.

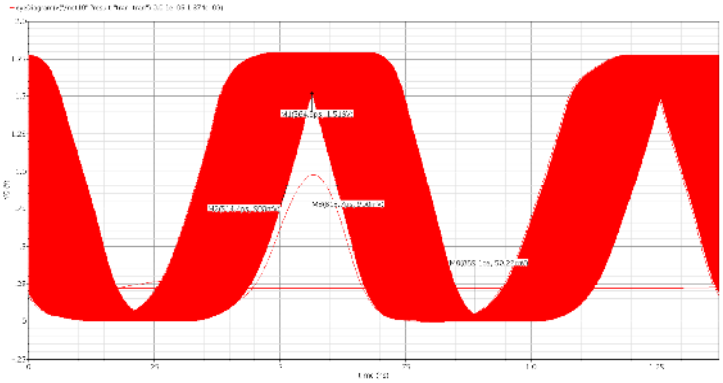

Figure 10. Eye diagram of the VCO output waveform at 1.456GHz when input is 1V (Contains approx. 708 cycles).

There is a time difference of 99.3ps at 50% of V_{DD}. V_{DD} values at top and bottom are 1.519V and 50.22mV respectively. The time jitter can still be made less by connecting a D flip flop at output of VCO. But we get half of the VCO output frequency. In this design we observed the maximum time jitter after D flip flop 3.1ps and 1.5ps for rising and falling edge respectively, and output frequency is from 173MHz to 1.2GHz.

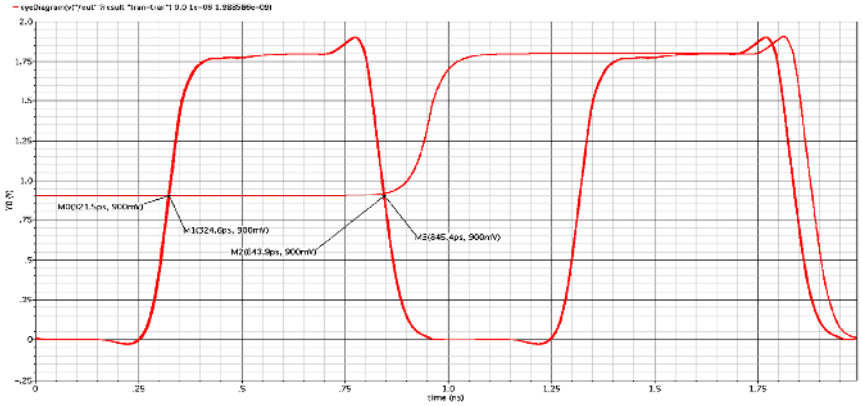

Figure 11. Jitter calculation after D Flip flop (Divide by 2).

6. CONCLUSIONS

The CSVCO circuit is designed and simulated using GPDK 180nm CMOS Technology. The CSVCO has frequency range from 53 MHz to 2.348 GHz and power consumption is 848µW. The jitter is improved by connecting a D Flip Flop (divide by 2). The supply voltage V_{DD} is 1.8V. The current starved oscillator gives a linear voltage controlled oscillations, which is useful for PLL upto a certain GHz frequency range.

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REFERENCES

[1] Floyd M Gardner, *Phase Lock Techniques*, 3rd ed., Wiley Interscience Publication, 2005.

[2] R. Jacob Baker. CMOS circuit design, Layout and simulation, John Wiley and Sons Inc, Publication, 2010.

[3] Paul R Gray, Paul J Hurst, Stephen H. Lewis, Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th Edition, John Wiley & Sons, Inc.

[4] Farid Golnaraghi, Benjamin C. Kuo, *Automatic Control Systems*, 9th Edition, John Wiley & Sons, Inc.

[5] Roland E. Best, *Phase-Locked Loops Design, Simulation and Applications*, 5th edition, McGraw-Hill Publications.

[6] William F. Egan, *Phase-Lock Basics*, John Wiley & Sons, Inc.

[7] Stanley Goldman, *Phase-Locked Loop Engineering Handbook for Integrated Circuits*, Artech House, Inc, 2007.

[8] Behzad Razavi, *RF Microelectronics*, Prentice Hall communication engineering series.

[9] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, International Edition, McGraw Hill publications, 2001.

[10] Cadence manual, 2004.

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