FPGA BASED HEARTBEATS MONITOR WITH FINGERTIP OPTICAL SENSOR

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ABSTRACT

The heart is an organ of human body which has a vital function, small abnormalities can have a big impact on the performance of the body. Heart disease is the number one cause of death in the world. Examination of the heart can be detected from blood flow in the fingertips, in order to obtain information about the number and rhythm of the heartbeat. This research aims to design and implement the FPGA board to monitor the heart rate with optical sensors.The results of this study are expected to facilitate the patient's medical team or independently in detecting heart health. The series is composed of blocks of sensors, signal conditioning block, the block pulse counter, block timer 10 seconds and blocks the viewer. Based on the test results of the 10 respondents with a variety of age and gender, has built a tool that the percentage error of 3.94%.

KEYWORDS

Heartbeat monitor, Xilinx ISE Webpack, FPGA, optical sensor

1. INTRODUCTION

The heart is an organ of human body which has a vital function, small abnormalities can have a big impact on the performance of the heart kita.Penyakit body is the number one cause of death in the world. Based on data from the World Health Organization (WHO), cardiovascular disease has reached 29% in the percentage of deaths in the world and 17 million people die every year due to heart and blood vessel disease throughout the world [3].

The development of medical instrumentation systems is growing rapidly along with the need for medical personnel to diagnose a patient and a medical examination. One medical instrumentation used for the examination of the heart is Electrocardiograph (ECG). ECG is a medical instrument that is commonly used by the medical team to detect heart rate and rhythm [6]. EKG can not be used independently by patients to detect a patient's pulse. In addition to the expensive costs for the procurement of ECG, ECG devices also require special skills to operate.

Along with the requirement in the design and manufacture of medical devices, digital electronics design technology is developing very rapidly, both in terms of hardware and software. Xilinx is one manufacturer that produces equipment or tools for modeling the design of digital systems. One product is in the form of a kit module board FPGA (Field Programmable Gate Array). FPGA is a programmable device that is composed of large modules independent logic that can be configured by the user who is connecting through the canals of programmable routing [4].

Field Programmable Gate Array (FPGA) has advantages of which can be configured by the End User, does not require the fabrication process, and the available solutions that support customized VLSI chip, so the logic circuit capable of implementing, instant manufacturring, very-low cost prototype. While FPGA product is also supported by the availability of the Xilinx ISE WebPack permograman language that is used as a GUI for the digital system design problems is desired.

Based on the above issues, this study will design a device that can detect heart rate by detecting the frequency of blood flow to the fingers automatically processed electronically using the module FPGA (Field Programable Gate Array). This research is expected to generate a heartbeat detector chip implementation can provide facilities for the medical and can be used independently by the user (patient) without the help of a doctor or paramedic.

2. ARCHITECTURE AND ITS IMPLEMENTATION

This research conducted several phases of hardware design, software design pelangkat, testing tools, and analysis to draw conclusions.

2.1 Hardware Design

The design of this tool consists of several circuit blocks are arranged into a single system heartbeats monitoring based on optical sensors, as shown in Figure 1.
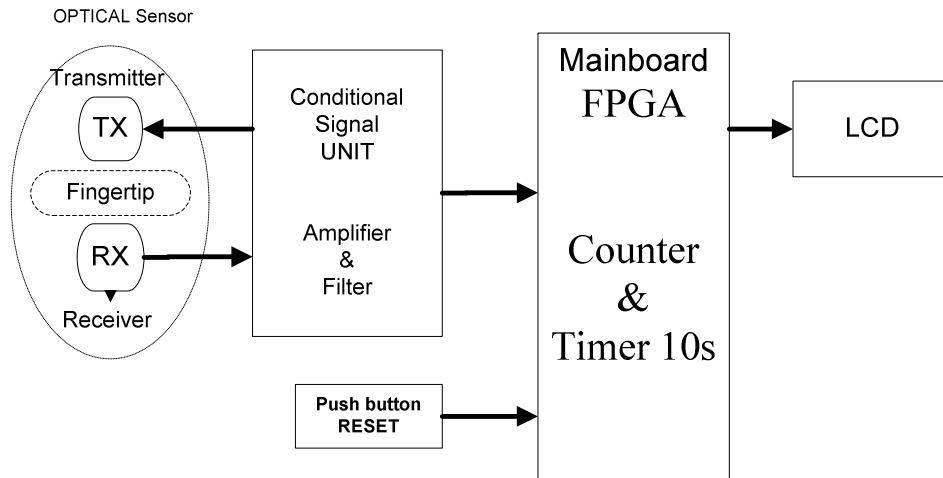

Figure 1. Block Diagram Tool Heartbeats Detection Based on Optical Sensors

2.1.1. Optical Sensor Unit

The sensor consists of a transmitter that emits infrared light (IR) and IR photo detector (photodiode) to act as a receiver. Construction sensor block shown in Figure 2. The use of optical sensors for process monitoring heart rate with fingertip illustrated as a figure 3.
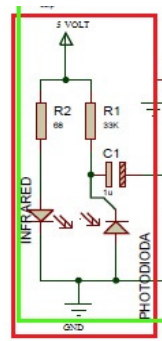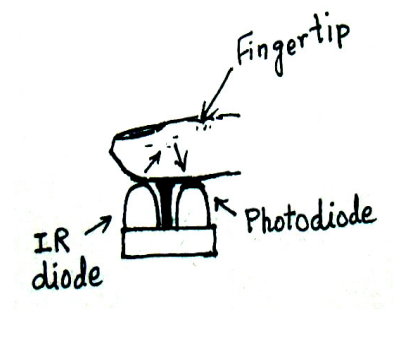
Figure 2. Optical sensor circuit

Figure 3. Ilustration fingertip to optical sensor

2.1.2. Conditional Signal Unit

The output signal of the sensor is very small and still a lot of noise. This signal before entering the pulse counter block should be done in conditioning, so signal that result this block is ready to be read or processed by the block counter. The signal conditioner block consists of a series of low pass filter and amplifier structure is shown as figure 4.
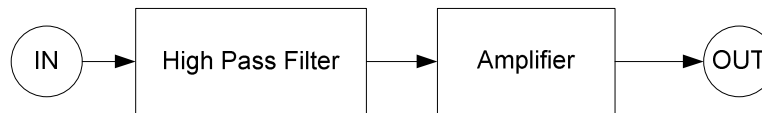

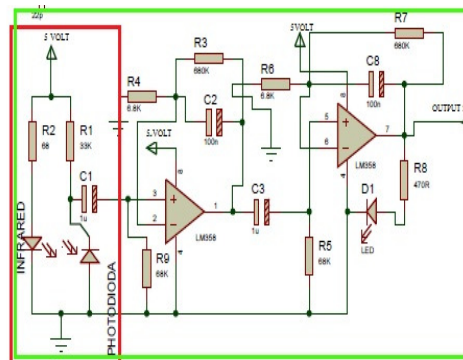Figure 4. Diagram Block of Conditional Signal Unit

Figure 5. Optical Sensor and Conditional Signal Circuits

2.1.3. Heart Counter Unit

This block is used to calculate the output signal generated by the signal conditioning block. Signals that represent a high rate, while the low signal represents the absence of heartbeat. So this block will calculate the amount of high signal.

The basic principle of this block as a series of counters. This block has three inputs namely are Clk signal, the signal In is connected to the output signal conditioning block and Enable signal (En) which is connected to the output signal at the timer block. The output of the pulse counter block form as 6-bit binary sequence (D5, D4, D3, D2, D1, D0). In this research, the pulse

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counter block is designed with programming languages Xlinx WebPack ISE. The design of the pulse counter block is shown as figure 6.
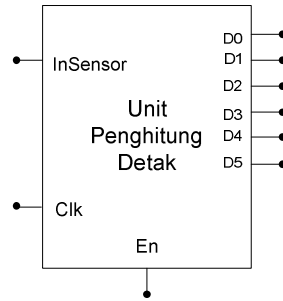

Figurer 6. Design of Heart Counter Unit

2.1.4. Timer 10s Unit

This block is designed for pulse counting process is done by calculating the input signal to the timer block rate for 10 seconds. The basic principle of the timer unit is a clock signal frequency divider circuit. The clock signal is taken from the internal oscillator signal frequency of 50 MHz on the FPGA module. In order to get a signal with a period of 20 seconds, then beat signal as a function of the timer must have a frequency of 50 mHz, by taking half the period of the high level. The output signal timer 10s unit to be input to the Enable signal (En) at the pulse counter block. The timer 10s unit is shown in Figure 7.
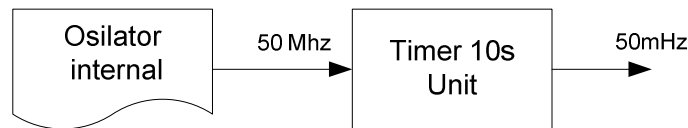

Figure 7. Diagram Block of Timer 10s

2.1.5. Display Unit

The Display unit that is used is the 6 Led (D5, D4, D3, D2, D1, D0) which represents the value of the output of the pulse counter block. In addition, the results of the calculation rate is also displayed with an LCD unit. This block already exists in the module of Spartan 3E FPGA Starter Kit [4], as shown in the figure 8.

Figure 8. Display of LED and LCD at FPGA Spartan 3E Starter Kit [4]

2.2. Designing of Programming Xilinx ISE Webpack

In this research, design of Xilinx ISE Webpack program done on the pulse counter block and block the timer 10s. The programming result, then applied to the module Field Programable Gate

Array (FPGA), through the implementation process. Output of this system is the number of heartbeat information in 1 minute, which known as beat permenit (bpm). Using of this system, in the process of beating the count is done for 10 seconds as the sample to calculate the 1 minute, so to show the heartbeat detection for 1 minute, required multiple of 6 constant number. Flowchart program of heartbeat monitoring device shown in figure 9.

Results from the VHDL programming of heartbeat monitorr has been simulated correctly, then the program is implemented on Spartan 3E FPGA board.
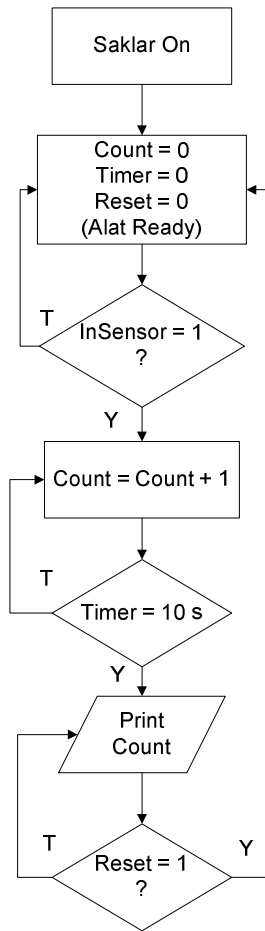
Figure 9. Flowchart of Heart Rate Monitoring VHDL Programming
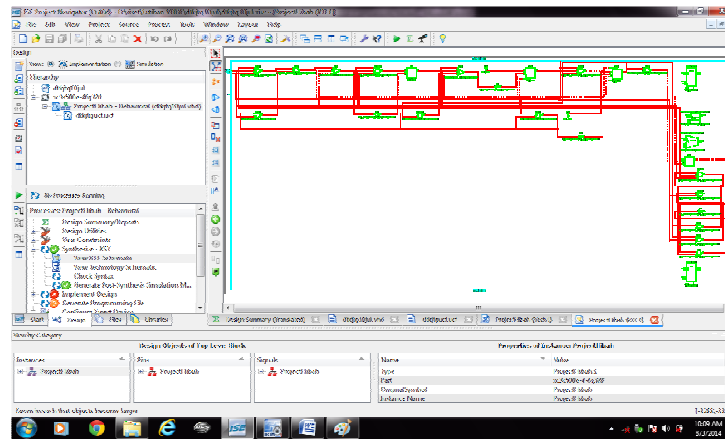
2.3. RTL Viewer

Figure 10. RTL Viewer Heartrate Monitor

After the process of synthesis and design implementation, next the process is VIEW RTL Schematic, as shown in the figure 10. This figure describes the gates configuration that represent the pulse counter and the timer 10s devices.

3. EXPERIMENTAL RESULT

3.1 Conditional Signal Output Testing

Based on Figure 11, can be explained that the heart rate signal measurement results using the oscilloscope at the output of the signal conditioner has a value of amplitude of 8.4 V, with a value of 800 ms period or frequency of 1.25 Hz.
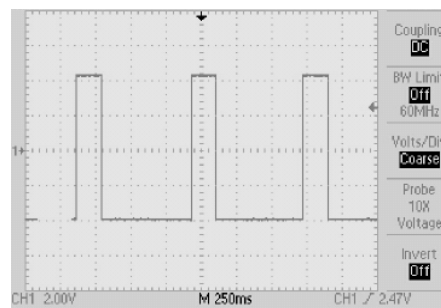

Figure 11. Display of output the signal conditioning block on the oscilloscope output

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3.2. Simulation Results Heartbeat Counters Block

Testing in this section is to observe the results display on the programming VHDL simulation with Xilinx Isim, as shown as Figure 12.
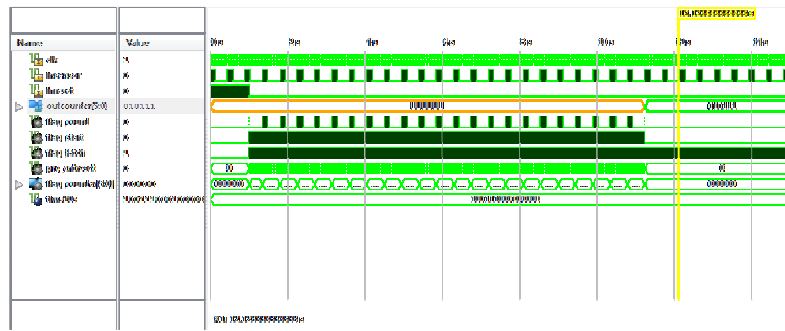
Figure 12. Display of simulation result

Figure 12 shows an example of simulation result Heartbeat Counters Block with a insensor input signal with a period of 450ms (1.33Hz). At the output outcounter generate data 010111b, which represents the beating of the time there are 23 counters for 10 seconds. So that the calculation results heartbeat (heart rate) for 23 x 6 = 138 bpm (beats perminute).

3.3 Testing Results of The Heartbeats Monitor Device

Testing is done by calculating the heart rate to some respondents. Based on the output pulse counter block built instrument (ha) compared with the measurement results using a fingertip pulse sensor oxymeter (ho) in units of bpm. Difference in outcome differences between the two devices, then calculated the percentage error (% Er) with the equation:

$$\%Er = \frac{|ha - ho|}{ho} x100\%$$

……………..……………………..(1)

Table 1: Testing results of the heartbeats monitor device

Responden	LED Condition FPGA						Heart Rate (bpm) LCD	Heart Rate (bpm) Oxymeter	Error (%)
	D5	D4	D3	D2	D1	DL0			
1	0	0	1	1	0	1	78	76	2,6
2	0	0	1	0	1	1	66	70	5,7
3	0	0	1	1	1	0	84	82	2,4
4	0	0	1	1	0	1	78	77	1,3
5	0	0	1	1	1	0	84	81	3,7
6	0	0	1	1	0	0	72	75	4
7	0	0	1	1	1	1	90	84	7,1
8	0	0	1	1	0	1	78	82	7,3
9	0	1	0	0	0	0	96	94	2,1
10	0	0	1	1	1	1	90	93	3,2

Table 1 shows the trial against six respondents. At trial respondent 1, the output of the gain block rate pengitung 001101b value as indicated by the LED flash is worth 1, and if the flame is not worth 001101b value 0 is equivalent to 13d. Furthermore, to get the heart rate measurement with units of beats per minute (bpm) needs to be multiplied by a constant 6 Thus, respondent 1 has a value of 13 x 6 = 78 bpm. The same was done for the other respondents. Measurement accuracy

in terms of percentage error is calculated using equation (1). Based on the test results in Table 1, it has been tested tool designed to measure the number of heartbeats to 10 respondents, has an error (Error) an average of 3.94%.

4. CONCLUSION

This research has successfully designed a heartbeat monitor circuit using the Xilinx ISE program WebPack 13.1. The series is composed of sensors block, signal conditioning block, pulse counter block, timer 10s unit and the display unit. Based on the test results of the 15 respondents, a tool designed to have a percentage error of 3.28%.

5. SUGESTION

a. In the testing process, the accuracy of the optical sensor is strongly influenced on laying / finger placement ujuag. So to overcome this required the manufacture of containers or the media, so the detection of blood flow in the fingertips can be precision quickly.
b. In the signal conditioning block in this research, design and manufacturing are still using electronic components. In further studies need to be developed to block the signal conditioner made with vhdl programming, thus forming sauté specific integrated circuits or ASICs known (Application-Specific Integrated Circuits)
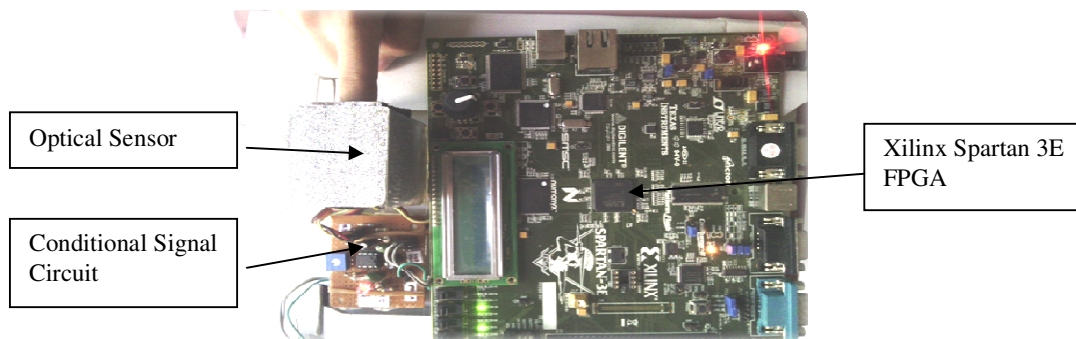

Figure 13. FPGA based heartbeats monitor circuit

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