A NEW DESIGN REUSE APPROACH FOR VOIP IMPLEMENTATION INTO FPSOCS AND ASICS

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ABSTRACT

The aim of this paper is to present a new design reuse approach for automatic generation of Voice over Internet protocol (VOIP) hardware description and implementation into FPSOCs and ASICs. Our motivation behind this work is justified by the following arguments: first, VOIP based System on chip (SOC) implementation is an emerging research and development area, where innovative applications can be implemented. Second, these systems are very complex and due to time to market pressure, there is a need to built platforms that help the designer to explore with different architectural possibilities and choose the circuit that best correspond to the specifications. Third, we aim to develop in hardware, design, methods and tools that are used in software like the MATLAB tool for VOIP implementation. To achieve our goal, the proposed design approach is based on a modular design of the VOIP architecture. The originality of our approach is the application of the design for reuse (DFR) and the design with reuse (DWR) concepts. To validate the approach, a case study of a SOC based on the OR1K processor is studied. We demonstrate that the proposed SoC architecture is reconfigurable, scalable and the final RTL code can be reused for any FPSOC or ASIC technology. As an example, Performances measures, in the VIRTEX-5 FPGA device family, and ASIC 65nm technology are shown through this paper.

KEYWORDS

Voice over IP, Systems on Chip, FPGA, FPSOC, ASIC, Design reuse

1. INTRODUCTION

The rapid progress in the semiconductor technology, in conformity with the Moors' law prediction, is offering to designers more integration capacity than they consume. This fact is well known under the name of ''design gap'' or ''design productivity problem'' [1]. Besides this, the very hard competition in electronic innovation is more and more constraining designers to reduce to the minimum the time of putting their product on the market ''time to market.'' To overcome this problem, and according to the International Technology Road Map for Semiconductors (ITRS) [2], three solutions are proposed:

- Exploitation of ''design reuse''
- Development of advanced methodologies and tools for the design and test, particularly using high abstraction levels
- Development of application specific platforms

These three solutions are complementary from each other. They aim to close the gap between what the semiconductor technology is offering in term of integration capacity, and what is practically possible to implement in silicon with current design methodologies and tools.
Subsequent to this progress in technology, VOIP has witnessed a great evolution since its introduction in the beginning of 1995. Ended, a huge diversity of VOIP solutions have been proposed, ranging from software applications based on general purpose processors and DSPs circuits to dedicated applications based on ASICs, FPSOCs and embedded systems [3-7]. The choice between one implementation style and another depends essentially on the target application field which can be either an enterprise VOIP system or a small office-home office VOIP system. The differences between these two implementation classes' reside principally in the capacity of the gateways, the flexibility, the scalability and the complexity of the hardware used. Aside these differences, there are common factors such as the quality of service and the power dissipation. Particularly, dedicated applications, share common features/constraints such as portability, area, speed and power dissipation. However, these systems are relatively complex, they require expertise in both hardware, software and algorithmic and thus involve multidisciplinary teams. The major problems are:

- Complexity and size of the project.
- Hardware and software partitioning between different tasks that execute the algorithm.
- IP cores must use a standard interface.
- The design effort is moved from the functionality of the circuit to communication between different IP cores in the SOC.
- Test of the whole SOC.
- Power management
- Physical and technological effects

In order to deal with these problems, designers need new concepts to handle the increased complexity inherent in these large chips. One such emerging concept is the application of design reuse to VOIP design.

In [8] the reuse concept has been applied in VOIP but in a software context. In [3-7] the SOC design of VOIP are presented. At our knowledge, theses chips are considered as intellectual property and thus there is no information how they are designed, which methodology and which platforms are used?

In [9], we presented hardware architecture of the VOIP Gateway. In this paper, we present an extended version in which guidelines to develop the reuse concept are outlined. Our motivation behind this work is justified by the following arguments: first, VOIP based System on chip (SOC) implementation is an emerging research and development area, where innovative applications can be implemented. Second, these systems are very complex and due to time to market pressure, there is a need to built platforms that help the designer to explore with different architectural possibilities and choose the circuit that best correspond to the specifications. Third, we aim to develop in hardware, design, methods and tools that are used in software like the MATLAB tool for VOIP implementation.

Section 2 gives basic concepts of design reuse, section 3 deals with the proposed design methodology. In section 4, the SOC gateway architecture is presented. In section 5, synthesis and implementation results are presented and finally a conclusion.

2. BASIC CONCEPTS

2.1 THE DESIGN REUSE CONCEPT

Design reuse presents specific challenges to the designer. But to be reusable, a design must first be usable: a robust and correct design. To achieve this goal, the design must fulfill the following requirements: well coded, well commented, well verified and well documented. In addition to the above requirements, there are some additional requirements for a design to be reused. These requirements are published in the Reuse Methodology Manual (RMM) [10]:

- Designed to solve a general problem: configuration
- Designed for use in multiple technologies: technology independence
- Designed for simulation with a variety of simulators: portability
- Designed with standard-based interfaces
- Verified independently of the chip in which it will be used
- Verified to a high level of confidence
- Fully documented

From the above requirements, it appears that to move from a simple design to a reusable design, an additional design effort is required.

Reuse, as a solution to the design productivity gap, has created a new branch in the semiconductors industry, called IP reuse business [11] as shown in Fig. 1

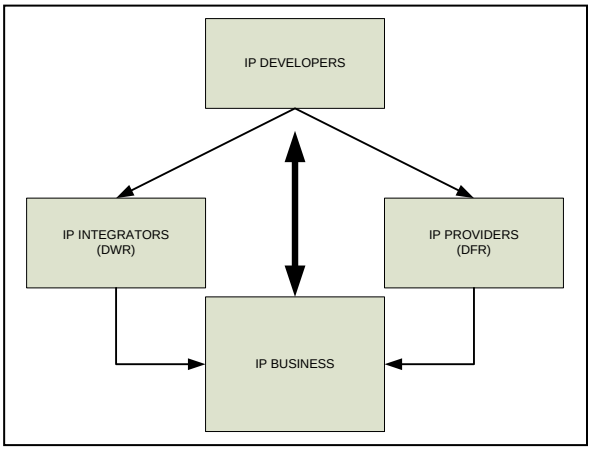

Figure 1. IP Business Model

There are three major players: IP providers/developers, IP integrators and IP tool developers.

- *IP providers/developers*: They supply libraries of IP components, including hard cores, soft cores and firm cores. The designer must plan design to supply an IP than can be reused. Thus, the term design for reuse (DFR) is used. Aspects of documentations, verification, quality assurance, standardization, maintenance, etc. are issues that must be solved in the DFR strategy.

- *IP integrators*: are typically designers/users of IPs supplied by IP providers. The term design with reuse (DWR) is used, because the design is done with predesigned and preverified IPs. The major issues that face IP integrators are exploration and exploitation of provided IPs, integration of theses IPs in a new design and a methodology of reuse and

standardization of the process of IP acquisition.• Tools developers: supply design tools to IP providers and integrators.

- *The Business model* is related to IP distribution service and trade.

2.2 VOICE OVER IP (VOIP)

Voice over IP had its starts in February 1995 when a manufacturer started marketing software that enabled a conventional computer equipped with a sound card, microphone and loudspeaker to phone another PC via the internet. Initially, the voice quality achieved was unsatisfactory but the principle behind it drew a great attention of public, thus the first area of application for VoIP: PC-to-PC was established. Subsequent to this introduction a number of manufacturers concentrated on developing similar software and consequently raised the question of compatibility among different systems. In 1996, the International Telecommunication Union responded by developing the H.323 standard. Afterwards, the focus was the possibility of placing long distance calls using voice over IP known as toll bypass; however this required setting up a connection between the telephone network (PSTN) and the data network, a task performed by so called Gateways [12]. The result has been additional application for VoIP including: PC-to-phone, Phone-to-PC and, when two gateways are used, Phone- to - phone communication. This last option was the catalyst in the establishment of a new provider group named ITSP (Internet Telephone ServiceProvider) that permits telephony over IP within the provider network using prepaid cards. To date, VoIP refers to the ability to transfer data and voice and also video on the single network. Figure 2 illustrates the basic operating principle of VoIP.

The human voice initially generates an analog signal.This signal is converted into a bit stream by an Analog/Digital (A/D) converter and then submitted to a multiple compression process. The Voice frames are integrated into a voice packet. First RTP (Real time protocol) packet with a 12 address byte header is created. Then an 8-byte UDP packet with the source and destination address is added. Finally, a 20 byte IP header containing source and destination gateway IP address is added.The packet is sent through the internet where routers ands switches examine the destination address. When the destination receives the packet, the packet goes through the reverse process for playback. A minimal VoIP implementation requires two functionalities. First, it should be able to connect to other VoIP phones and, second, voice data should be carried by the Internet. The first requirement is fulfilled by using signaling. The second one is achieved by using speech coding algorithms.

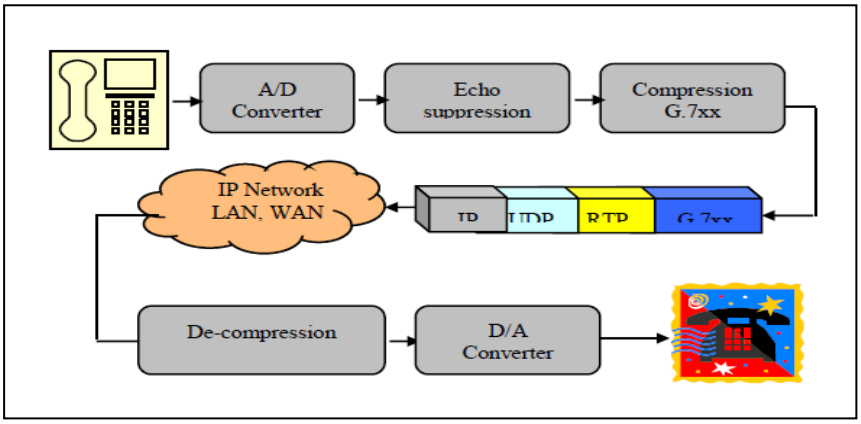

Figure 2 Principle of VoIP

The speech coding allows the reduction of transmission speech signal and communication channels to a limited bandwidth. The bandwidth of a transmission must be minimized while maintaining the quality of voice signal. Most codecs are algorithms, used to reduce the bit rate of speech data incredibly, while maintaining the voice quality. The most commonly used codecs in VOIP systems are: G.711PCM [14], G.726 [15], ADPCM, G.729 LD-CELP [16], and G. 729/G.729a CS-ACELP [17]. PCM and ADPCM belong to the family of so called waveform codecs. These codec simply analyze the input signal without any knowledge of the source. Most of these codecs work in time domain, like PCM. These codecs offer high quality speech at a low computational complexity. But if we try to get the bit rate below 16 kbps the quality decreases tremendously. To get the bit rate really down another approach is necessary. Source coders need to know the characteristics about the input being coded. Out of these characteristics a model of the source is made. When an input is encoded the source coder tries to extract the exact parameters of this model from the input. Then these parameters and a two state excitation is transmitted. These codec can simply transport the pure informational content of a speech sample and not the voice itself. Their big advantage is that they operate with bit rates as low as 2.4 kbit/s. Hybrid codec try to combine the advantages of waveform codec, which is good quality, with the advantages of the source codec that is low bit rate. To get the best excitation signal all possible waveforms are tested and the one with the least error is then chosen. This involves a very high computational complexity for every analysis frame. The low bit rate codecs usually involve a high computational complexity and a delay and the waveform codecs have the advantage of low delay and excellent quality. In Table 1 there is an overview of the quality of the different codecs according to the Mean Opinion Score. This score is derived from a large number of listeners who rated the quality of the played sample with a score from excellent (5) to bad (1). It should be understood that the various coding methods vary in the levels of complexity, delay characteristics and quality.

Table1. Characteristics of the most coding algorithms

Coding algorithm		Bandwith (Kbps)	Algorithmic Delay (ms)	Complexity (MIPS)	MOS
G.711	**PCM**	64	0.125	0	4.3
G.726	**ADPCM**	16-40	0.125	6.5	2.0-4.3
G.728	**LD-CELP**	16	0.625	37.5	4.1
G7.29	**CSACELP**	8	10	17	3.4

3. VOIP System on chip DESIGN METHODOLOGY BASED ON DFR AND DWR

In this section a design methodology is proposed based on the design for reuse (DFR) and the design with reuse (DWR) concepts. To achieve this goal some design rules must be applied to the code of the VOIP architecture according to the Reuse Methodology Manual (RMM).

3.1 APPLICATION OF THE RMM DESIGN RULES

As shown in section 2, to be reusable, the VOIP hardware design must fulfil the following rules which are based on the RMM:

3.1.1 CONFIGURATION

Configuration can be obtained by exploiting the programmability nature of FPGA devices, by integrating different descriptions of codec algorithms, communication networks and processors for the same architecture.

3.1.2 TECHNOLOGY INDEPENDENCE

This rule can be satisfied by using a high level description language such as the VHDL [18], VERILOG [19] or System-C [20] for the VOIP architecture description.

3.1.3 PORTABILITY

In order to satisfy this rule, the generated ANN code must be portable for synthesis and simulation. ISE foundation [21], CADENCE [22] and ModelSim [23] are the tools used for synthesis and simulation respectively. This choice is justified by the wide use of these tools and by their availability at our level.

3.1.4 DESIGNED WITH STANDARD INTERFACES

The IEEE standard interfaces signals declarations are used to achieve this rule.

3.1.5 VERIFIED WITH A HIGH LEVEL OF CONFIDENCE

To this end, a prototype must be realised in an FPGA prototyping board.

3.1.6 ENTIRELY DOCUMENTED IN TERMS OF APPLICATION AND RESTRICTIONS

To achieve this goal, VOIP project documentation must be delivered at the end of the project.

3.2 THE PROPOSED DESIGN REUSE METHODOLOGY

The proposed design reuse strategy is shown in Figure 3 as a process of Flow. In this figure, the methodology is based on a top-down design approach in which the user/designer is guided step by step in the design process of the VOIP gateway architecture. First, the user/designer is asked to choose the codec compression algorithm to be implemented and the number of lines that can be implemented. The compression algorithms that can be supported are the PCM G711 with a-law and µ-law, the G722 and G728 audio codec. The number of lines is related to the number of Ethernet that can be incorporated. In the next step, a VERILOG code description of the SOC gateway architecture is generated. Before synthesis, functional simulation is required. Then, the VERILOG code is passed through a synthesis tool that performs Register transfer level (RTL) synthesis and optimization according to the target FPGA device family and under speed/area constraints. The result is a file ready for placement and routing. At this level, verification is also required before power analysis and then downloading the programming file into the FPGA prototyping board. To help the user/designer, documentation is available at each level of the design. It is to be mentioned that all the cores used in this design are downloaded from the OpenCores web site and are free of charge [24].

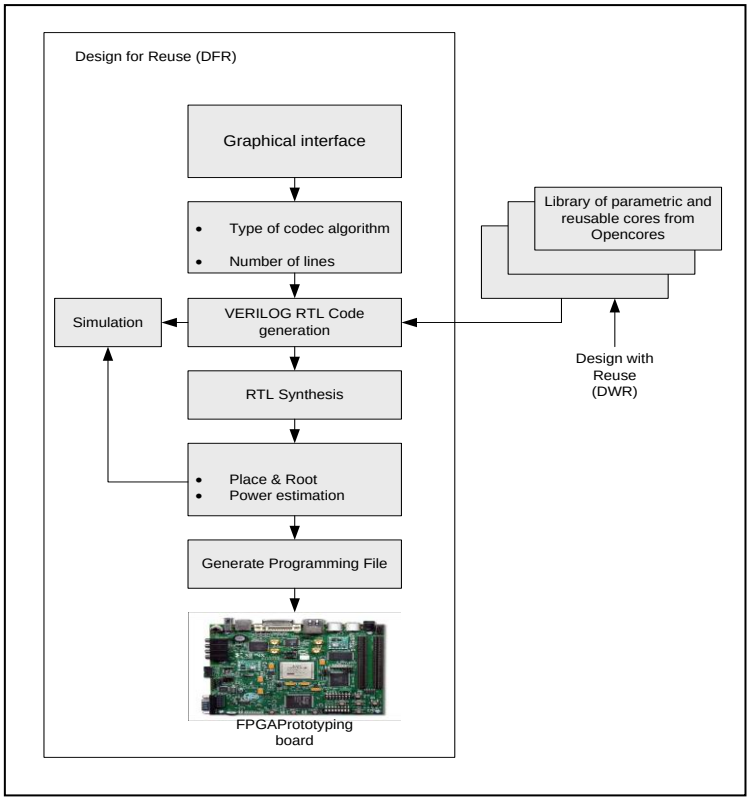

Figure 3 Proposed design reuse methodology

As shown in Figure In our approach the design reuse methodology is exploited at two different levels. First, by using the cores of OpenCores library, we exploit the Design with Reuse concept (DWR). Second, by creating a generic SOC gateway architecture, in which the cores can be modified, we can say that SOC-gateway is designed for Reuse (DFR).

4. THE VOIP ARCHITECTURE

Figure 4 shows the proposed gateway architecture which is mainly based on theOpenRisc OR1200_V3 processor, a debug unit for debugging purpose, an Universal Asynchronous Receiver Transmitter (UART), an audio codec for voice compression, an AC97 audio controller,a standard MAC/Ethernet, a flash memory for internal boot, a DDR2 memory for embedded application and other interfaces for LCD display, keypad, Speaker and handsets. The cores are connected through the WISHBONE bus interface.

Figure 5 shows the OR1200-V3 internal architecture and Figure 6 shows the WISHBONE bus interconnection schema.

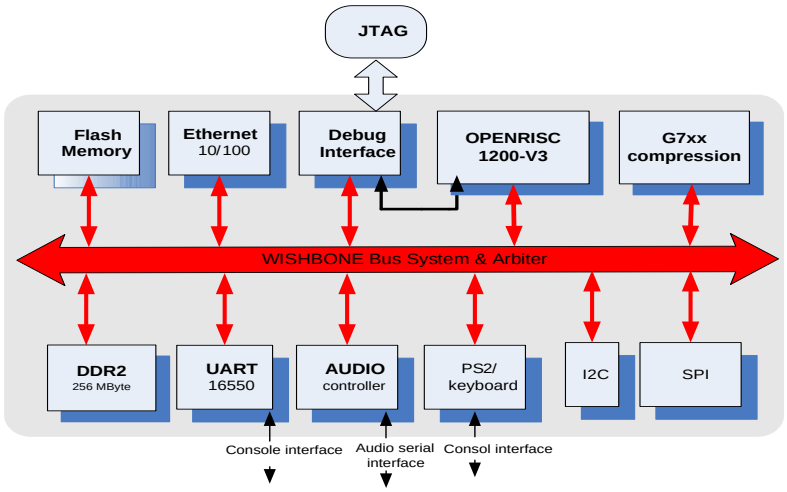

Figure 4 The VOIP Gateway general architecture

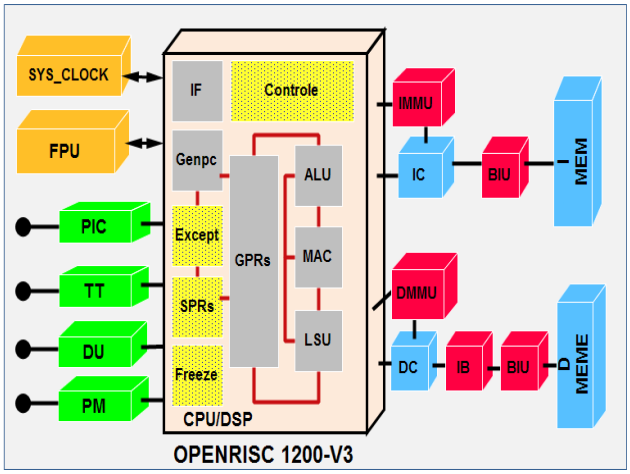

Figure 5. OR1200 Architecture

As shown in Figure 5, The OpenRisc 1200-V3 is a 32/64-bit RISC synthesizable processor with Harvard micro-architecture, 5 stage pipeline. It is developed and managed by a team of developers at OpenCores. An overview of the OpenRisc 1200-V3 architecture is illustrated in figure 5. The new features compared to the older version is that it support the new implementation of IEEE 754 compliant single precision FPU, also new instruction/data register MMU is added for embedded Linux distribution.

The WISHBONE bus interface uses a MASTER/SLAVE architecture. Some signals are specific to the master core, others to the slave one and there are common signals shared between the master and the slave. The MASTER interface could be on a microprocessor IP core, and the SLAVE interface could be on a serial I/O port (Figure 6).

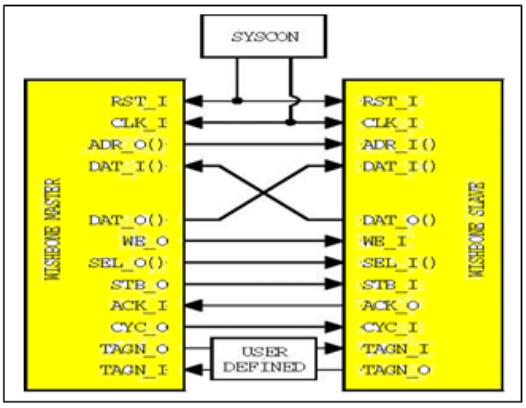

Figure 6. WISHBONE interconnect schema

In this architecture the WISHBONE uses the shared bus interconnection schema, thus a MASTER initiates a bus cycle to a target SLAVE. The target SLAVE then participates in one or more bus cycles with the MASTER. An arbiter determines when a MASTER may gain access to the shared bus. The main advantage to this technique is that shared interconnection systems are relatively compact. Generally, it requires fewer logic gates and routing resources than other configurations such as the cross bar switch configuration. It is to be noticed that the wishbone bus can supports up to 8 masters and 16 slaves as well as 4 priority level. This characteristic can be explored to add more Ethernets and codec cores to boost the capacity and scalability of the gateway.

5. SYNTHESIS AND IMPLEMENTATION RESULTS

Our first implementation is a SOC that integrates the G711 algorithm, one MAC/Ethernet, the Openrisc-V3 processor, a debug unit, the UART circuit, the AC97 audio controller, a flash memory, a DDR2, I2C, SPI and PS2 keyboard.de. We performed synthesis and physical implementation using the Xilinx ISE design tool [19]. The whole architecture is mapped into the Xilinx FPGA VIRTEX 5 ML501 FPGA. Table 2 shows the synthesis results. Mainly, the SOC occupies 52% of the FPGA in term of slice LUT, 42% of IOBs, 60% of bloc memory, 8% of integrated DSP and 16% of PLLs. Table 3 shows the power dissipation in each FPGA module. Mainly, the total estimated power is 4.3 Watt. It is to be mentioned that IOs blocs and leakage currents constitute the major source of power consumption. Another source of power consumption is the PLL module. In the other hand the DSP module consumption is zero. This is because the DSP integrates only few logics and is not really well exploited in this architecture. Figure 7 shows the final FPSOC layout. It is clear that for other algorithm configurations, if more Ethernet cores are integrated, a migration to another FPGA device with more resources is necessary. Figure 8 shows the VOIP ASIC layout using the Faraday 65nm technology.

Table 2 Synthesis results

Device Utilization Summary (estimated values)			
LogicUtilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	15098	28800	52%
Number of bondedIOBs	185	440	42%
Number of Block RAM/FIFO	29	48	60%
Number of DCM_ADVs	1	12	8%
Number of DSP48Es	4	48	8%
Number of PLL_ADVs	1	6	16%

Table 3 Power estimation

On Chip	Power
Clocks	0.291
Logic	0.006
Signals	0.011
BRAMs	0.015
DSPs	0.000
PLL	0.112
DCMs	0.094
IOs	3.209
Leakage	0.590
Total	4.328

6. CONCLUSION

We have presented a design reuse approach for hardware implementation of complex architectures such as VOIP systems. By adopting a design reuse methodology, we demonstrated that the architecture is reconfigurable and scalable. Key features of this architecture are: the integration of different kind of compression algorithms, the possibility to add or remove the number of lines which related to the MAC/Ehernet circuit and the final RTL code can be mapped into FPGA or ASIC devices. This work is still under progress especially regarding the ASIC. As future work, we aim first to optimize the architecture to get better performances. Also, we project to enrich the library by adding other processors and cores.

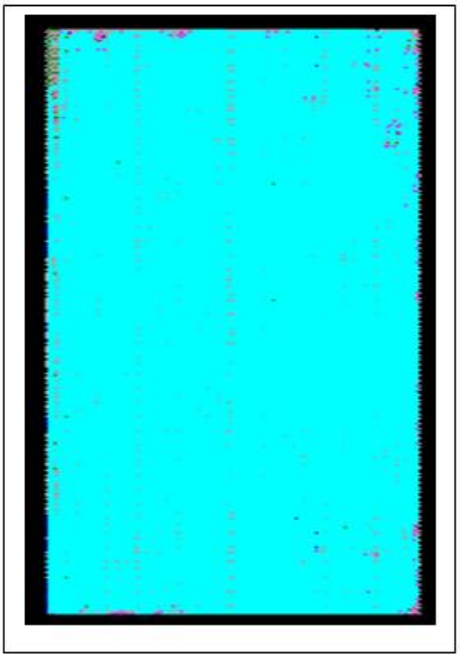

Figure 7 Final FPGA layout

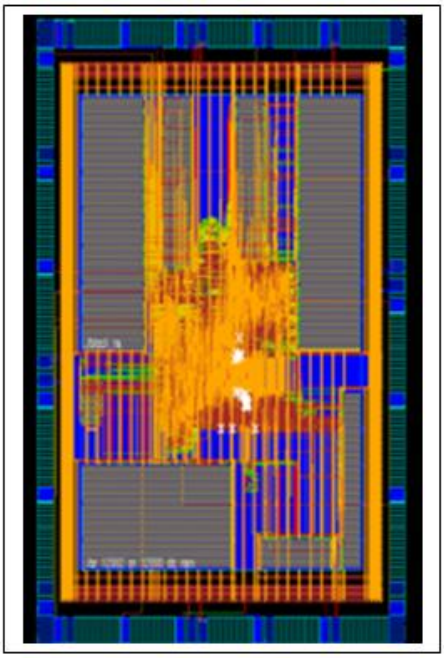

Figure 8 ASIC layout

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