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DESIGN AND SIMULATION OF CMOS OTA WITH 1.0 V, 55db GAIN & 5PF LOAD

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ABSTRACT

Design of very large scale analog integrated circuit (analog VLSI) is very much complex and requires much compromising nature to achieve application specific objective. With maximizing the efforts to reduce power consumption and to reduce W/L ratio, the analog integrated circuit industry is constantly developing smaller power supplies. Now days, challenges of analog integrated circuit designer are to make block of small power supplies with little or no reduction in performance. The CMOS OTA is designed in 25.5nm CMOS technology with 1.0V power supply to observe the configurations. In design of CMOS OTA TANNER EDA TOOL is used. Coding and simulation is done in T-Spice and layout is prepared in L-Edit. D.C analysis, A.C analysis, slew rate and analysis of transient response have been done in T-Spice. Waveforms are observed in W-Edit.

KEYWORDS

DRC, Net list, Slew Rate, Transconductance Amplifier

1. INTRODUCTION

The importance of analog circuits using low supply voltage is enormously increasing in last decades. Especially large component densities demands lower power consumption [2]. The power consumption can be minimized either by reducing the supply voltage or gate oxide thickness (Tox). If Tox is reduced, tolerance of the CMOS device for high gate voltage is also reduced. Therefore reasonable method for minimizing power consumption is to reduce power supply.

CMOS elements are useful building blocks for the design of many analog and analog-digital signal processing systems. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Because of these characteristics, the vast majority of modern integrated circuit manufacturing is on CMOS processes.

Operational Transconductance Amplifiers are important building block in many analog systems. These analog systems often require low power, fast settling time and high dynamic range. The CMOS Operational Transconductance Amplifier (OTA) is a unique device with characteristics particularly suited to applications viz. multiplexing, amplitude modulation, analog multiplication, gain control, switching circuitry and comparators.

2. DESIGN OF OTA

2.1. Low voltage and low power amplifier design

In low-voltage design, the main consideration is to maintain the output swing as higher as possible. This can be achieved when no cascading transistors can be used in the output stage. For minimum power consumption, the number of current branches should be minimized. So the current mirror amplifier is best suited for low-power low-voltage amplifier [1].

2.2. Current Mirror Amplifier

The circuit in which output current is forced to equal the input current is said to be a current mirror circuit. It is special case of constant current bias. An advantage of current mirror circuits is that it takes fewer components, simple to design and easy to fabricate.

2.3. Parameter require for designing CMOS OTA

1) Slew rate
2) Common-mode input range (ICMR)
3) Common-mode rejection ratio (CMRR)
4) Power supply rejection ratio (PSRR)
5) Voltage Gain

2.4. Design Specification

$V_{dd} = -V_{ss} = 1.0$ V, SR $\geq$ 10V/µs, C_L=5pF, a small signal differential voltage gain of 55db, -1.5$\leq$ ICMR $\leq$ 2V and $P_{diss} \leq$ 1mW

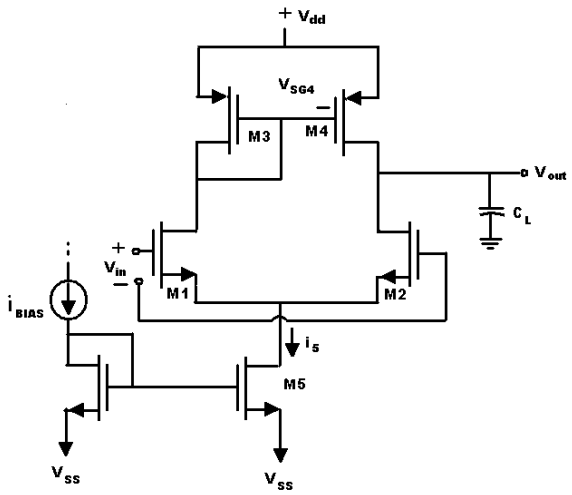

Figure 1. Design of CMOS OTA

2.5 MATLAB Code for extraction of designing parameter

V_{dd} = input ('enter the value of V_{dd} = ');
SR = input ('enter the value of slew rate SR =');

C_L = input ('enter the value of slew rate C_L=');

$I_5 = SR*C_L$
P_{diss} = input ('enter the value of power diss. P_{diss}');
V_{ss} = input ('enter the value of $V_{ss} = -V_{dd}$ =');
.....
.....
Y_n = input ('enter the value of Y_n =');
Y_p = input ('enter the value of Y_p =');
.....
$R_{out} = 2/((Y_n + Y_p)*I5)$;
V_{in} = input ('enter the value of Vin = ');
.....
$V_{sg3} = V_{dd} - V_{in} + V_{tn}$
K_p = input ('enter the value of K_p = ');
K_n = input ('enter the value of K_n = ');
$W_3/L_3 = I_5 / (K_p*(V_{sg3}-0.7)*(V_{sg3}-0.7))$
Av = input ('enter the value of Av = ');
$W_1/L_1 = ((Av)^2*(Y_n+Y_p)^2*I_5/2)/(2*K_n)$;
$V_{gs} = sqrt((I_5/K_n* W_1/L_1))+0.7$;
$V_{ds5} = V_{in}-V_{ss}-V_{gs}$;
$W_5/L_5 = sqrt((2*I_5)/K_n*(V_{ds}5)^2)$;

3. LAYOUT AND VERIFICATION CONSIDERATION

Layout should be verified with design rule viz. Design Rule Check (DRC) and Layout Versus Schematic (LVS).

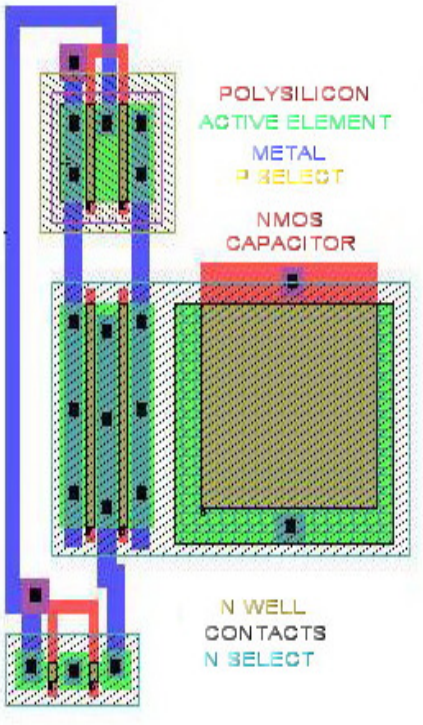

Figure 2. Layout of CMOS OTA in 25.5nm

3.1 Layout Versus Schematic (LVS) Summary (Extracted code from layout)

2 1 C=5.0147962p
* C7 PLUS MINUS (49.5 -45 91 -11.5)

M6 5 3 4 11 NMOS L=2n W= 56n AD=45.25p PD=28n AS=21p PS=14n
* M6 DRAIN GATE SOURCE BULK (23 -73.5 25 -70.5)
M5 4 3 3 11 NMOS L=2n W=56n AD=21p PD=14n AS=45.25p PS=28n
* M5 DRAIN GATE SOURCE BULK (13 -73.5 15 -70.5)
M4 6 10 5 11 NMOS L=2n W=58n AD=222p PD=86n AS=111p PS=43n
* M4 DRAIN GATE SOURCE BULK (30 -48.5 32 -11.5)
M3 5 9 7 11 NMOS L=2n W=58n AD=111p PD=43n AS=222p PS=86n
* M3 DRAIN GATE SOURCE BULK (22 -48.5 24 -11.5)
M2 3 7 7 8 PMOS L=2n W=51n AD=48p PD=22n AS=96p PS=44n
* M2 DRAIN GATE SOURCE BULK (22 5 24 21)
M1 6 7 3 8 PMOS L=2n W=51n AD=96p PD=44n AS=48p PS=22n
* M1 DRAIN GATE SOURCE BULK (30 5 32 21)

* Total Nodes: 11
* Total Elements: 7
* Total Number of Shorted Elements not written to the SPICE file: 0
* Extract Elapsed Time: 0 seconds
.END

Table 1. Summary of transistors in figure 1

Sr.No	Transistor Variable	W(n)	L(n)	W/L ratio
1	W_1/L_1	51	2	25.5
2	W_2/L_2	51	2	25.5
3	W_3/L_3	58	2	29
4	W_4/L_4	58	2	29
5	W_5/L_5	56	2	28
6	W_6/L_6	56	2	28

4. SIMULATION RESULT

4.1. Simulation in T-spice

T-Spice Pro is part of a complete integrated circuit design tool suite for layout, verification and simulation offered by Tanner EDA.
1) T-Spice: Analog / digital circuit simulator
2) W-Edit: Waveform viewer

AC Analysis
Perform AC analysis to characterize the circuit's dependence on small-signal input frequency.

.ac {lin|oct|dec} num start stop [sweep info] [analysis name=name]
DC Analysis

Perform DC transfer analysis to study the voltage or current at one set of points in a circuit as a function of the voltage or current at another set of points.

.dc info [sweep] info [sweep] info

4.2. Different Types of Simulation

4.2.1. DC characteristic

.DC VID -2.5V 2.5V 0.5V
.TF V(5) VID
.PRINT DC V(5)
.END

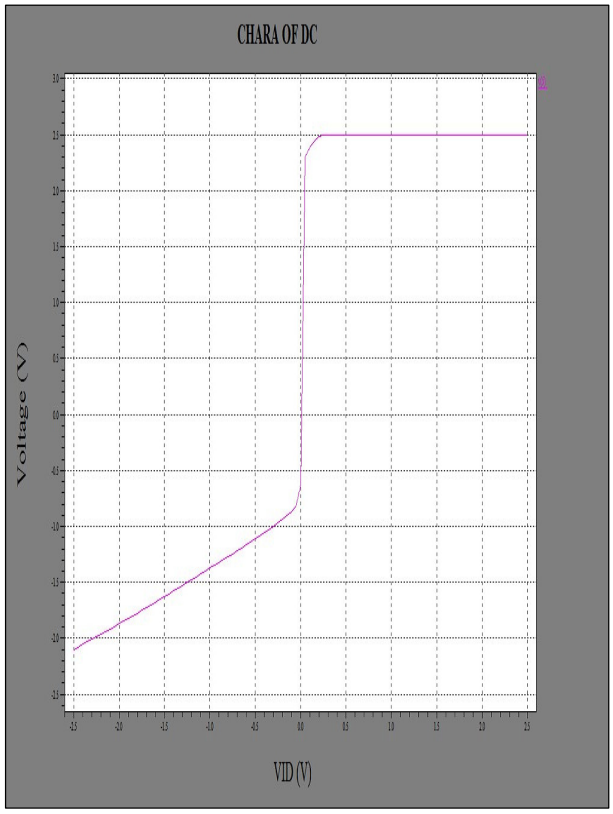

Figure 3. DC Characteristic of CMOS OTA

4.2.2. Slew Rate

VIN2 1 0 PWL (0,-3V 10US,-3V 10.505US, 3V 25US, 3V 25.505US,-3V 1S,-3V)
VIN1 2 0 PWL (0,-3V 10US,-3V 10.505US, 3V 25US, 3V 25.505US,-3V 1S,-3V)
.TRAN .1NS 40US
.PRINT V (5) V (1)
.PROBE
.END
From waveform of slew rate = (10-(-10))/.5µs = 40 V/µs

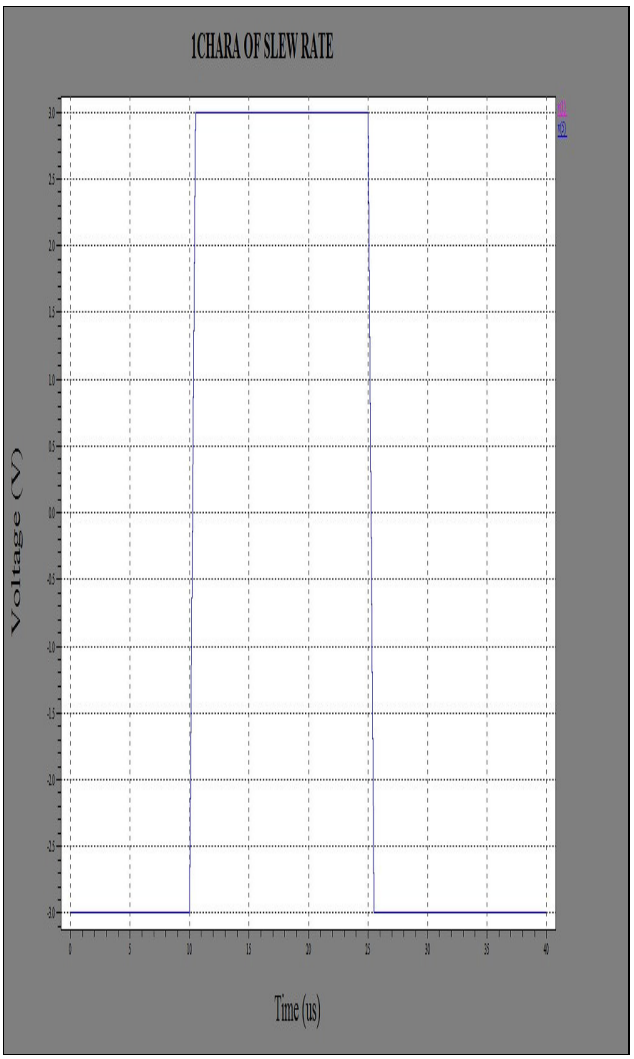

Figure 4. Slew Rate Analysis

4.2.3. AC characteristic

.AC DEC 5 0.1HZ 1MegHZ
.TF V(5) VID
.PRINT AC V(5) VP(5) VID
.PROBE

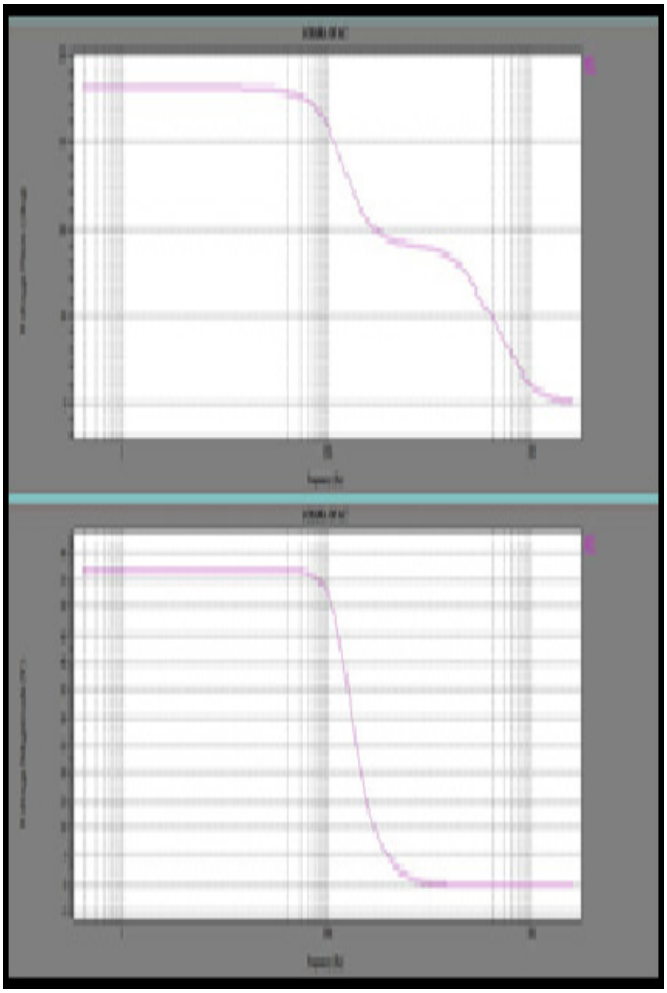

Figure 5. AC Characteristic of CMOS OTA

5. FUTURE WORK

The OTA layout con be further optimized to take up less space and also to get better symmetry. We will make layout of viz. Telescopic, Folded-Cascode and Two-stage CMOS OTA. We will compare their characteristics like gain, Speed, Power, Noise and Swing [1].

6. APPLICATIONS

IC CA3080A

IC CA3080A is especially suited for many low frequencies, low-power four-quadrant multiplier applications. The basic multiplier circuit is particularly useful for waveform generation, double balanced modulation, and other signal processing applications, where low-power consumption is essential and accuracy requirements are moderate. We can make the astable multi vibrator, monostable multi vibrator and peak detector [11].

IC OPA2662

It is dual, wide band Operational Transconductance Amplifier. The OPA2662 is a versatile driver device for ultra wide-band systems, including high-resolution video, RF and IF circuitry, communications and test equipment [11].

CMOS OTA is used in following application like,

1) LED and LASER diode driver
2) High current video buffer or line driver
3) RF output stage driver
4) High density disk drives

7. CONCLUSION

Simulations show the output is reliable up to about 10MHz, which is sufficient to find the 3dB bandwidth of the OTA. Structure of CMOS OTA is simple and is used as compare to ordinary op-amp because its output is a current. We can retrieve information about gain margin and phase margin. According to that we can retrieve information about pole and stability of the design.

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