THE QUANTIZED DIFFERENTIAL COMPARATOR IN FLASH ANALOG TO DIGITAL CONVERTER DESIGN

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ABSTRACT

This paper proposes a Flash Analog to Digital Convsrter design based on the use of a Quantized Differential Comparator. The formulation explores the use of a systematically incorporated input offset voltage in a differential amplifier for quantizing the reference voltages necessary for Flash ADC architectures, thus eliminating the need for a passive resistor array for the purpose. This work is an attempt to extend the TIQ method, which uses systematic sizing of devices in a conventional CMOS inverter to accomplish the same. The formulation allows very small voltage comparison and complete elimination of resistor ladder circuit. The design has been carried out for the TSMC 0.18u technology at MOSIS.

KEYWORDS

TIQ, Analog to Digital Converter.

1. INTRODUCTION

The flash type Analog to Digital converter architecture is the most attractive solution for high speed Analog to Digital converter designs, but from a power dissipation and area perspective it is not efficient for the resolution of more than 8 bits. As long as the resolution level is kept small, the comparator count will be reasonable, and its offsets are not critical. Therefore the comparator structure is the most critical part in full-flash type architectures.

Some of the problems of the conventional comparator structures used in A/D designs can be listed as follows [1]:

1. large transistor area for higher accuracy
2. DC bias requirement
3. charge injection errors
4. metastability errors
5. high power consumption
6. Resistor or capacitor array requirement.

The Threshold Inverter Quantizer (TIQ), based on systematic transistor sizing of a CMOS inverter in a full-flash scheme, eliminates the resistor array implementation of conventional comparator array flash designs [1,2]. Therefore no static power consumption is required for quantizing the analog input signal, making the idea very attractive for battery-powered applications.

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However there are five main disadvantages of the TIQ approach [1]:

1. It is a single ended structure.
2. It requires 2^n-1 different area sized quantizer designs.
3. It requires a separate 5V reference power supply voltage for analog part only due to poor power supply rejection ratio.
4. It has slight changes in linearity measures (DNL, INL) and the maximum analog signal range due to process parameter variations. These problems can easily be handled by front end signal conditioning circuit.
5. It requires S/H at the analog input to increase the performance and to reduce the power consumption during metastable stage.

The comparator is the most important part in the ADC architectures. It's role is to convert input voltage V_{in} into logic '1' or '0' by comparing the reference voltage V_{ref} with V_{in}. If V_{in} is greater than V_{ref} the comparator output voltage is '1' else it is '0'.

The TIQ comparator uses two cascaded inverters as comparators for high speed and low power consumption. Mathematically, the midpoint voltage V_m is given by,

$V_m=(r(V_{dd}-|V_{tp}|)+V_{tn}) / (1+r)$ with $r=(K_p/K_n)^{1/2}$

where V_{tp} and V_{tn} represent the threshold voltages of the PMOS and NMOS devices respectively [2]. At the first inverter, the analog input signal quantization level is set by V_m, depending on the W/L ratios of the PMOS and NMOS. The second inverter is used to increase voltage gain and to prevent an unbalanced propagation delay.

The TIQ flash ADC requires 2^n-1 different size comparators, so it is required to effectively find their sizes to correctly implement the TIQ comparators. However choosing the needed V_m from many candidates for comparators and generating the selected comparators with a custom layout are difficult jobs. For example, a 10-bit flash ADC would need 1023 TIQ comparators, too many for manual layout designs, while other ADCs use a single comparator design and simply duplicate it for 2^n-1 times. However, a customized program has been developed [2] that automatically generates the TIQ comparators with an optimal selection approach.

A CMOS inverter consists of one PMOS and one NMOS transistor, with the inverter switching threshold voltage, depending upon the transistor sizes. If the length of both the PMOS and NMOS are fixed, then different inverter threshold voltages can be obtained by simply varying the transistor widths. There are two design methods for the TIQ comparator for the V_m values. One method, called the Random Size Variation (RSV) technique, can obtain the 2^n-1 reference voltages by selecting the inverter width from the full range of 3-D surface without considering the relation of adjacent comparators. The other method, called the Systematic Size Variation (SSV) technique, considers the relation of comparators in selection of the inverter size[2].

Perhaps the most critical issue for the Threshold Inverter (TI) comparator based ADC is the process variation [3]. One solution is to add a programmable pre-amplifier to the analog input of the ADC to dynamically fine-tune the offset, gain, and linearity. Another solution is to perform digital signal processing on the ADC output to correct the offset, gain, and linearity. Authors suggest second solution for system-on-chip applications where a processor is already on the same chip with ADC.

The thermometer code-to-binary code encoder has become the bottleneck of the ultra-high speed flash ADCs. In [4] the authors presented the fat tree thermometer code-to-binary code encoder that is highly suitable for the ultra-high speed flash ADCs. The simulation and the implementation results show that the fat tree encoder outperforms the commonly used ROM

encoder in terms of speed and power for the 6-bit flash ADC case. The speed is improved by almost a factor of 2 when using the fat tree encoder, which in fact demonstrates the fat tree encoder, is an effective solution for the bottleneck problem in ultra-high speed ADCs.

Using the concept of TIQ comparator technique and fat tree encoder, a 6-bit and 8-bit flash ADC were designed with 0.07µm CMOS technology and 0.7V power supply voltage [5].

A power and Resolution Adaptive Flash Analog-to-Digital Converter (PRA-ADC) enables exponential power reduction with linear resolution reduction [6]. Unused parallel voltage comparators are switched to standby mode. PRA-ADC is capable of operating at 5-bit, 6-bit, 7-bit and 8-bit precision. PRA-ADC can operate at higher speed and consumes less power when it operates at a lower resolution. The PRA-ADC feature is highly desirable in many wireless mobile applications. For example, the strength of a radio frequency signal varies greatly depending on geographic location. Optimally, the ADC resolution can be reduced upon the reception of strong signal, and the resolution can be increased upon the reception of weak signal. Substantial reduction of power consumption at lower resolution prolongs the battery-powered operation.

The High-Speed Power and Resolution Adaptive Flash ADC (HSPRA-ADC) [7] utilizes an encoder design which significantly improves its speed and minimizes the chip area over the PRA-ADC design. The HSPRA-ADC is smaller in size since it uses a single encoder plus minimal extra logic for conversion at different resolutions. The HSPRA-ADC utilizes an encoder design, which is based on the Fat Tree Encoder Design. This design is based on the flash ADC architecture, Threshold Inverter Quantization (TIQ) ADC.

This paper presents 6-bit flash Analog to Digital Converter at 0.18u technology, which uses TIQ concept for the generation of the reference voltages in Quantized Differential Comparator.

2. A 6-BIT FLASH ADC

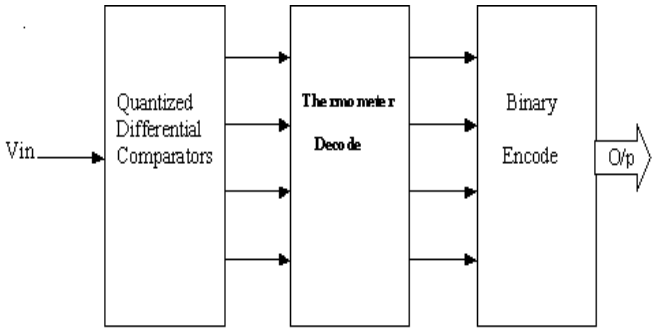

Figure 1. Block diagram of the proposed Flash ADC

Figure 1. shows the block diagram of proposed Flash ADC. The proposed flash ADC features the Quantized Differential Comparator technique for low voltage applications. The comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the Quantized Differential Comparator. The output of the comparator is '1' or '0' depending on applied input voltage.

In the conventional differential voltage comparator [8, 9], the transistor sizes are matched and the input V_b is taken from V_{ref} generated by resistor ladder circuit. Therefore all the comparators of n-bit flash ADC are identical. On the other hand, we use different transistor sizes of the transistor M2 of the differential pair to create an offset voltage in Quantized Differential Comparator. In addition, the voltages at V_2 and V_b are constants and input voltage is applied to the V_1 terminal (Figure 2). The desired internal reference voltage is generated with this intentional mismatch in the differential pair. On account of this, 2^n-1 different sizes of comparators are needed for the flash ADC implementation. To get sharp Voltage Transfer Characteristic (VTC) curves the inverter is used at the output of the differential amplifier.

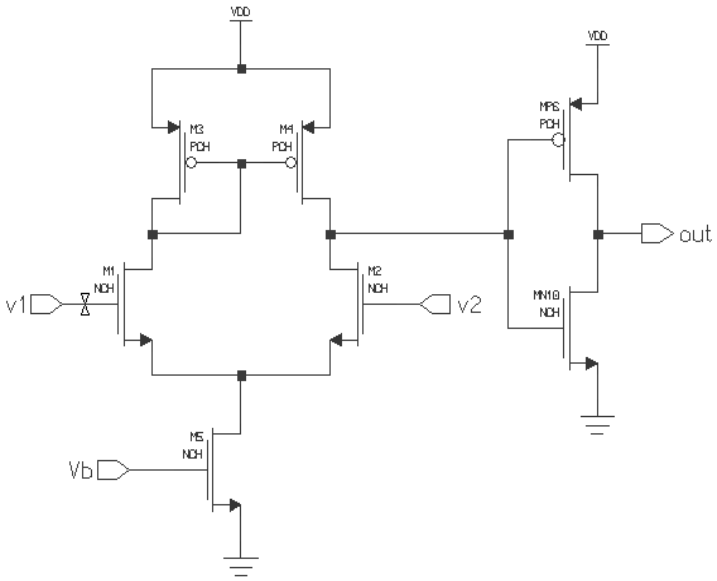

Figure 2. Quantized Differential Comparator

To design n-bit flash ADC, one needs 2^n-1 equal quantization voltages, and those many number of Quantized Differential Comparators. A PERL code has been developed to generate the different sizes of transistors for different reference voltages of the comparators and the device sizes have been picked up from the data generated to match the requirements.

After the comparators produce a thermometer code, the thermometer decode is used, which generates 1-out-of-n code, using XOR logic. The CMOS XOR gate circuit diagram is as shown in Figure 3.

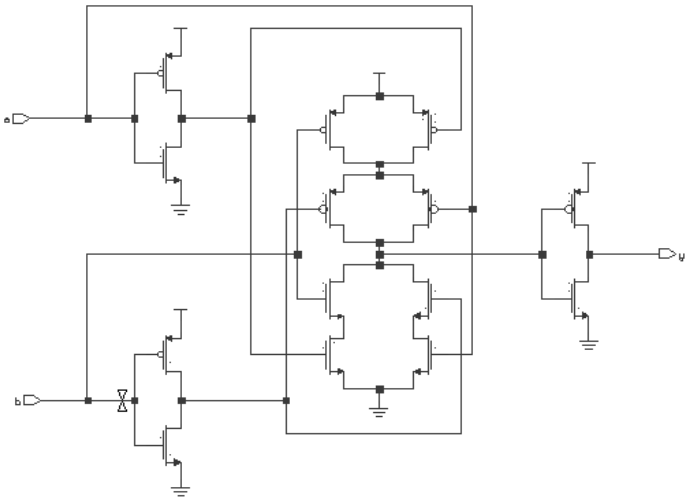

Figure 3. CMOS XOR gate circuit diagram

To convert 1-out-of-n code to binary code, a NOR based ROM array is used [10]. An optimized (with respect to transistor sizes) NOR-based ROM array circuit has been developed to achieve high-speed conversion. Only one row is activated at a time by raising its voltage to V_{dd}, while all other rows are held at low voltage level. If an active transistor exists at the cross point of column and the selected row, the column voltage is pulled down to the logic low level by that transistor. If no active transistor exists at the cross point, the column voltage is pulled high by the PMOS load device. Thus, a logic "1" bit is stored as the absence of an active transistor, while a logic "0" bit is stored as the presence of an active transistor at the cross point. A three-bit version of the NOR based ROM array incorporated is shown in Figure 4.

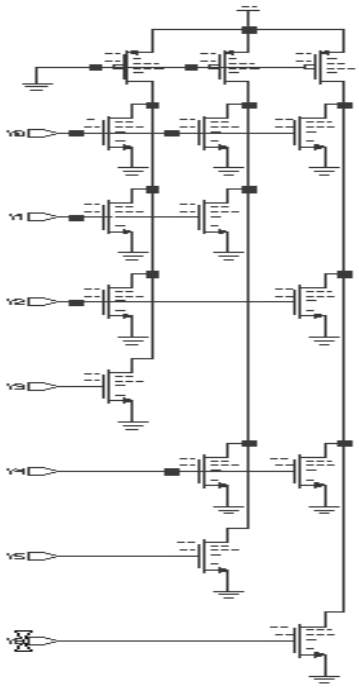

Figure 4. Three bit version of the NOR based ROM array

3. SYSTEM PERFORMANCE

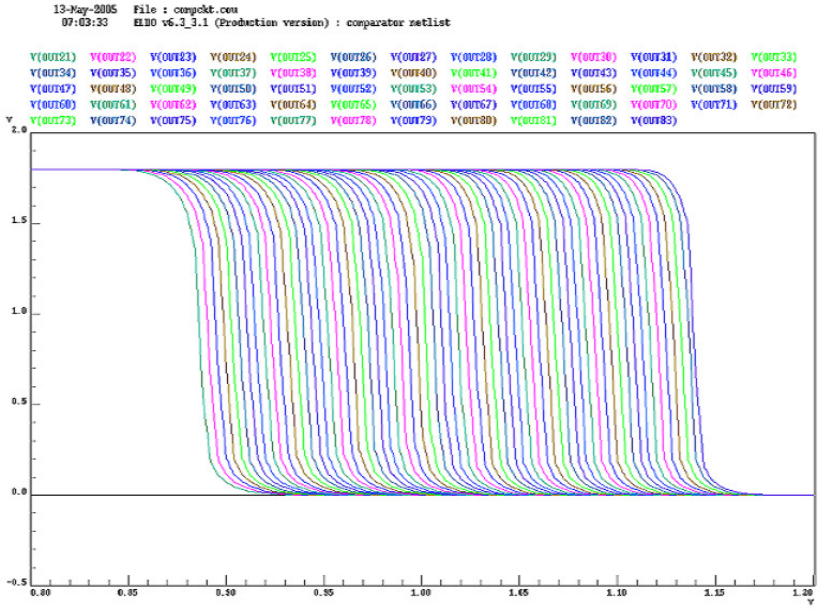

Figure 5. VTC of the Quantized Differential Comparator

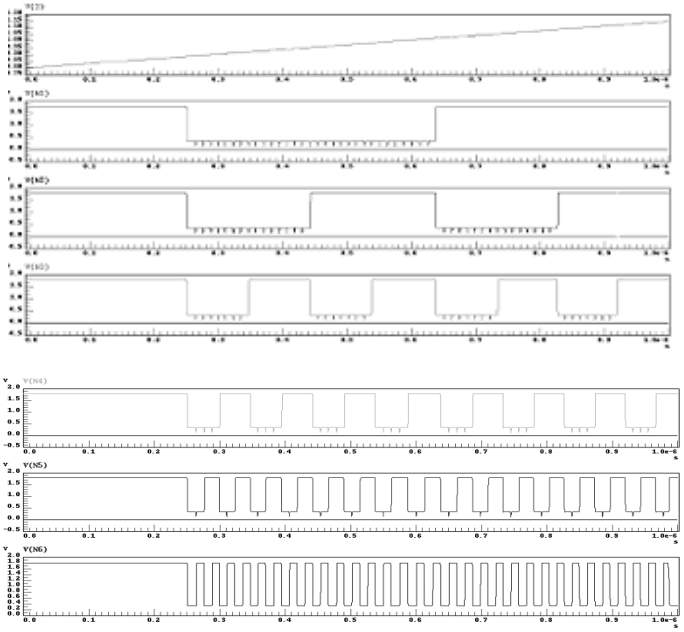

Figure 6. Simulation results for the 6-bit flash ADC using the Quantized Differential Comparator

The proposed Quantized comparator has been designed for TSMC 0.18u technology using Mentor Graphics Back-end Suite (DA_IC, EldoSpice). The proposed approach has been validated through extensive SPICE simulations. The VTC of a set of quantized comparators is shown in figure 5, clearly depicting the desired step changes in the switching voltage of the comparator. A 6-bit flash ADC employing the Quantized Differential Comparator has been designed to further validate the proposed approach. Simulation results for the same shown in Figure 6, clearly illustrate the feasibility of the proposed approach. Table. 1 lists the total number of transistors used in various functional modules of the proposed design. Table 2 gives the characterization of proposed ADC and Table 3 the comparison with other ADCs.

Table. 1. Transistor counts in the proposed design

Functional Module	No. of Transistors
1. Comparator	504
2. XOR Logic	870
3. ROM array	198
Total No. of transistors	1572

Table 2. ADC characteristics

Parameter	Specification
Architecture	Flash
Resolution	6-bit
Power Supply	1.8V
Technology	0.18µm
Power Dissipation	36.98mw
DNL	+0.02/-0.024 LSB
INL	+0.018/-0.024 LSB

The process variation is the most critical issue of the comparator. The solution is to perform digital signal processing on the ADC output to correct the offset, gain, and linearity.

Table 3. The proposed ADC power dissipation in comparison to other ADCs in the literature.

ADCs	Technology	Power Dissipation
Proposed	CMOS 0.18µm	36.98mW
6-bit TIQ[11]	CMOS 0.25 µm	59.91mW
6-bit Flash[12]	GaAs 0.5 µm	970mW
6-bt Flash[13]	CMOS 0.6 µm	380mW
4-bit Flash[14]	GaAs 0.8 µm	185.6mW
6-bit Flash[15]	CMOS 0.4 µm	400mW
8-bit Pipelne[16]	CMOS 0.6 µm	395mW
6-bit Flash[17]	CMOS 0.6 µm	330mW
4-bit Flash[18]	SiGe BiCMOS (160 GHz)	4.5W
5-bit Flash[19]	0.13 µm	120mW

4. CONCLUSION

A flash ADC design, based on a Quantized Differential Comparator approach has been proposed. The design has been carried out for 0.18u technology and validated through SPICE simulation circuit topologies and simulation results have been presented. Since the reference voltages are generated internally the power dissipation is reduced. DC simulation results show that there is a improvement in DNL and INL values. The results obtained are encouraging and indicate that the proposed approach can be promising one for battery driven applications such as SOCs.

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