HIGH PERFORMANCE VOLTAGE CONTROLLED OSCILLATOR (VCO) USING 65NM VLSI TECHNOLOGY

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ABSTRACT

CMOS" refers to both a particular style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry in VLSI dissipates less power when static, and is denser than other implementations having the same functionality. As this advantage has grown and become more important, CMOS processes and variants for VLSI have come to dominate, so that the vast majority of modern integrated circuit manufacturing is on VLSI technology processes. A key circuit use in modern communication is voltage control oscillator VCO's output is a AC waveform whose frequency is dependent upon the input voltages. In today's wireless communication system, greater maximum frequency required by the VCO w.r.t. to the digital phones that use these circuit, low power consumption, small size & low fabrication cost are important design factor. The layout of VCO which is develop by us is a modified design of high performance VCO .This is a optimum design for use in industries at 65 nm VLSI technology . In the estimated design ,more emphases is given on power consumption, layout design and many more. This report is a brief study of high performance VCO on 65 nm VLSI technology to achieve some objectives as mention above

KEYWORDS

Voltage controlled oscillator, 65nm, VLSI Technology, microwind 3.1, high performance.

1. INTRODUCTION

The electronics industry has achieved a phenomenal growth over the last two decades, mainly due to the rapid advances in integration technologies, large-scale systems design - in short, due to the advent of VLSI [1]. The number of applications of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been rising steadily, and at a very fast pace. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field[2].

A new MOS model, called BSIM4, has been introduced in 2000[3]. A simplified version of this model is supported by Microwind 3.1, and recommended for ultra-deep submicron technology simulation. The role of oscillators is to create a periodic logic or analog signal with a stable and predictable frequency. Oscillators are required to generate the carrying signals for radio frequency transmission, but also for the main clocks of processors. The output is equal to the input, and the phase difference is equal to one fourth of the period ($\pi/2$) according to the phase Detector principles

The voltage controlled oscillator (VCO) generates a clock with a controllable frequency[4] . The VCO is commonly used for clock generation in phase lock loop circuits . The clock may vary typically by +/-50% of its central frequency. The current-starved inverter chain uses a voltage control Vcontrol to modify the current that flows in the N1, P1 branch as shown in fig .4. The current through N1 is mirrored by N2, N3 and N4. The same current flows in P1. The current through P1 is mirrored by P2, P2, and P4. Consequently, the change in Vcontrol induces a global change in the inverter currents, and acts directly, the delay.

The Software microwind 3.1used in paper allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. You can gain or access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

2. TECHNOLOGY OVERVIEW & DESIGN ISSUES

In the technology overview and design issues, first of all ring oscillator is described. Then simple voltage controlled oscillator is described using cmos transistor .The disadvantage occurs in simple voltage controlled oscillator are overcome in High performance oscillator.

2.1. Ring Oscillator

The role of oscillators is to create a periodic logic or analog signal with a stable and predictable frequency. Oscillators are required to generate the carrying signals for radio frequency transmission, but also the main clocks of processors[4].

The ring oscillator is a very simple oscillator circuit, based on the switching delay existing between the input and output of an inverter. If we connect an odd chain of inverters, we obtain a natural oscillation, with a period which corresponds roughly to the number of elementary delays per gate. The fastest oscillation is obtained with 3 inverters (One single inverter connected to itself does not oscillate). The usual implementation consists in a series of five up to one hundred chained inverters. Usually, one inverter in the chain is replaced by a NAND gate to enable the oscillation. Fallowing fig .1shows a ring oscillator based on an odd number of inverters

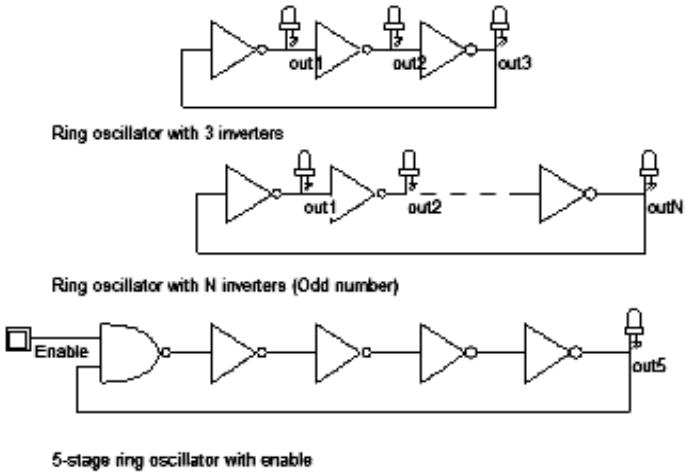

Figure 1. A ring oscillator based on an odd number of inverters

The main problem of this type of oscillators is the very strong dependence of the output frequency on virtually all process parameters and operating conditions. As an example, the power supply voltage VDD has a very significant importance on the oscillating frequency.

The oscillation frequency of the ring oscillator is neither stable, nor controllable, and even not precisely predictable, as it is based on the switching characteristics of logic gates which may fluctuate +/-20%.

In Microwind, the threshold and mobility parameters are varying with a *Normal* distribution <Gloss>, with a typical variation of 10%. The normal distribution of the threshold voltage *Vt* corresponds to a density of probability fallowing the equation.

$$f_{Vt} = \frac{1}{\sqrt{2\pi}\sigma} e^{\frac{(Vt-Vt_0)^2}{2\sigma^2}}$$

where

f is the density of probability

σ=0.1 (Equivalent to 10% typical fluctuation of the parameter)

Vt0=typical threshold voltage (0.4V)

Vt= threshold value (V)

The aspect of *f* versus *Vt* is given in figure.2.

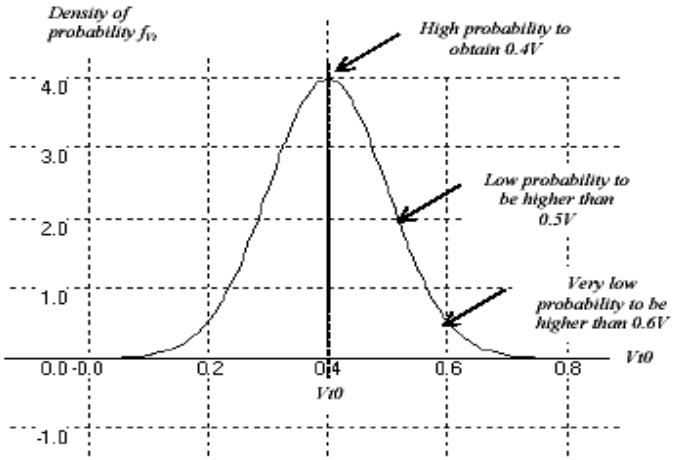

Figure 2. The normal distribution of Vt, with a typical variation of 10%

2.2. The Voltage Controlled Oscillator

The voltage controlled oscillator (VCO) generates a clock with a controllable frequency[5]. The VCO shown in fig.3 is commonly used for clock generation in phase lock

loop circuits. The clock may vary typically by +/-50% of its central frequency. The current-starved inverter chain uses a voltage control Vcontrol to modify the current that flows in the N1,P1 branch. The current through N1 is mirrored by N2, N3 and N4. The same current flows in P1. The current through P1 is mirrored by P2, P2 and P4. Consequently, the change in Vcontrol induces a global change in the inverter currents, and acts directly on the delay. Usually more than 3 inverters are in the loop. A higher odd number of stages are commonly implemented, depending on the target oscillating frequency and consumption constraints.

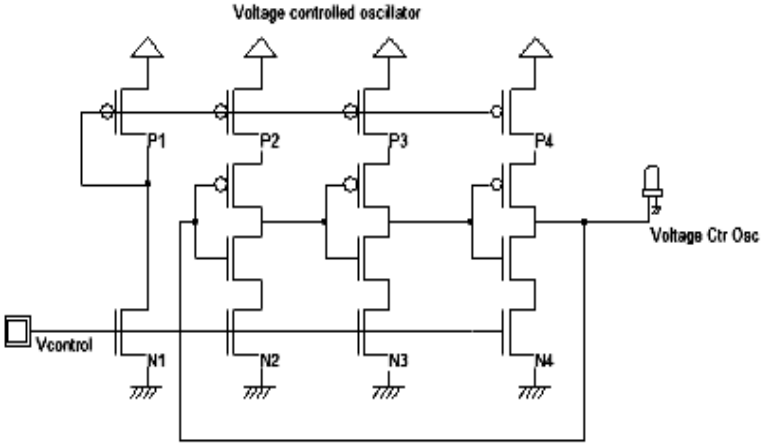

Figure 3. Schematic diagram of a voltage controlled oscillator

2.3. High Performance Voltage Controlled Oscillator

A voltage controlled oscillator with good linearity is shown in fig.4. This circuit has been implemented in several test-chips with successful results in 0.8, 0.35 down to 0.18µm technologies. The principle of this VCO is a delay cell with linear delay dependence on the control voltage [Bendhia]. The delay cell consists of a p-channel MOS in series, controlled by *Vcontrol*, and a pull-down n-channel MOS, controlled by *Vplage*. The delay dependence on *Vcontrol* is almost linear for the fall edge. The key point is to design an inverter just after the delay cell with a very low commutation point *Vc*. The rise edge is almost unchanged. To delay both the rise and fall edge of the oscillator, two delay cells are connected, as shown in the schematic diagram.

The layout of the VCO is a little unusual due to the needs for a very low commutation point for the inverter situated immediately after the delay cells. This is done by implementing a large n-channel MOS with high drive capabilities and a tiny p-channel MOS with low drive capabilities using microwind 3.1 version.

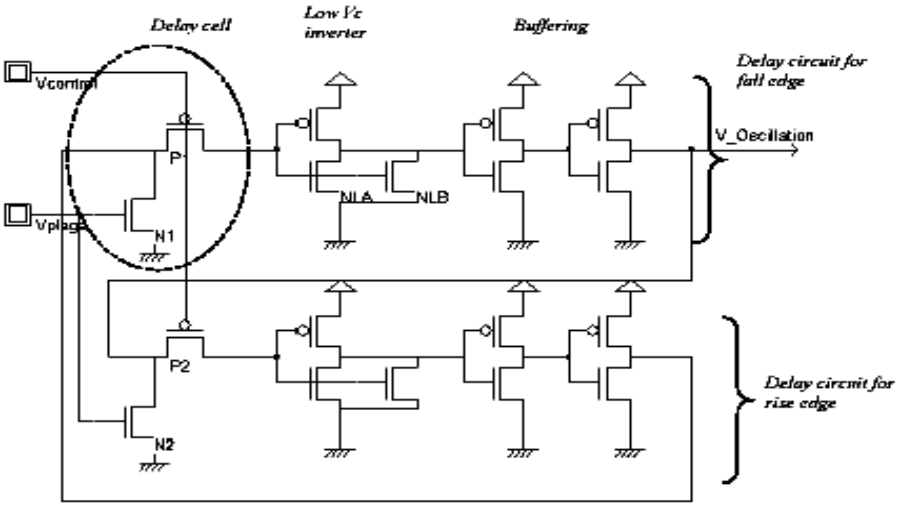

Figure 4. Schematic diagram of high performance VCO

The fallowing figure.5 shows a layout of a high –performance VCO using 65nm VLSI technology using BSIM4 transistor.

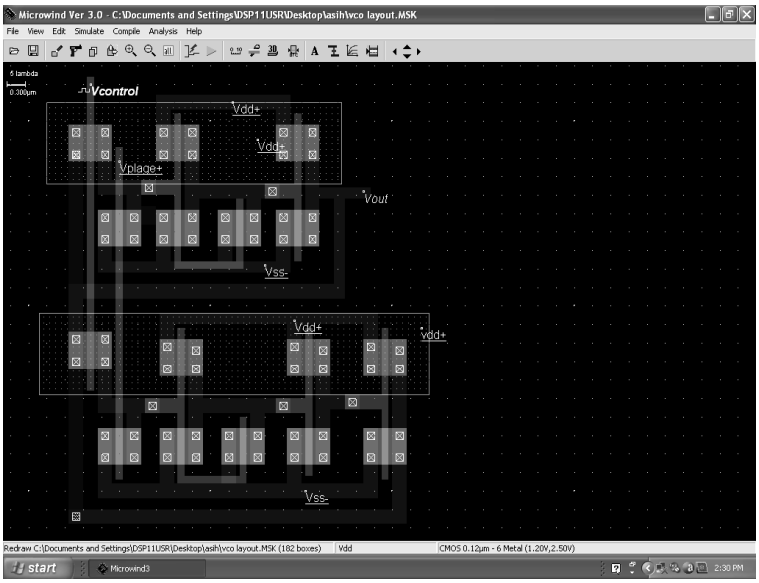

Figure.5. The layout implementation of a high performance VCO circuit

3. SIMULATION SETUP

This paper describes the improvement related to the CMOS 65 nm technology and the implementation of this technology in Microwind 3. For technology mode 65nm[4], effective

gate length is 25nm with metal gate and SiON gate dielectric. There may exist several variants of the 65-nm process technology. One corresponds to the highest possible speed, at the price of a very high leakage current. This technology is called “High speed” as it is dedicated to applications for which the highest speed is the primary objective: fast microprocessors, fast DSP, etc. The Software Microwind 3.0 used in paper allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

4. EXPERIMENTAL RESULTS

The simulation of a high performance VCO circuit is given in fallowing fig. 6 .This shows the simulation of a high performance VCO circuit ,frequency verses time .The frequency is 9.44GHz. for 0.106 nsec.

The quasi-linear dependence of the oscillating frequency on the input voltage control is observed within the range 0.6V.

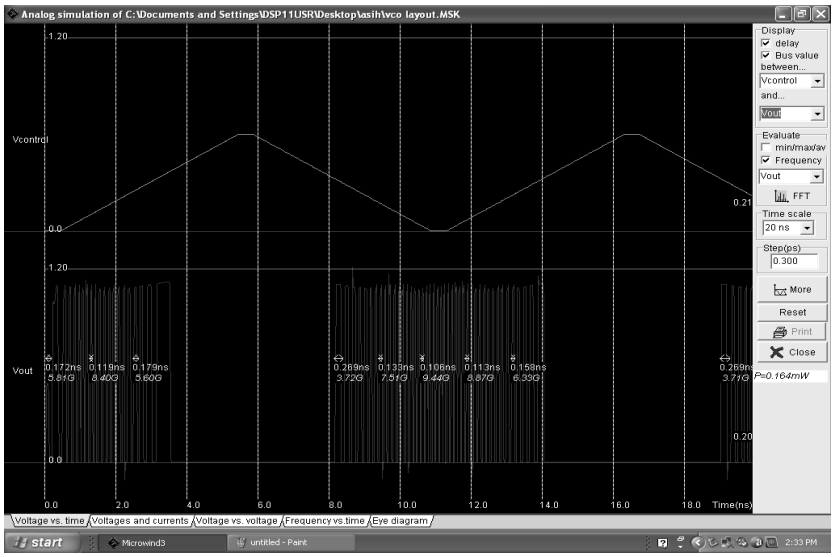

Figure 6. The layout simulation of a high performance VCO circuit, frequency verses time

The layout simulation of a high performance VCO circuit, voltage verses current and voltage verses voltage is shown in fig.7 & fig .8 respectively.

Although not displayed in the simulation, the voltage of Vplage has a strong influence on the oscillating frequency range. A high value of Vplage (Close to VDD) corresponds to a high frequency oscillation, while a low value (Close to the threshold voltage Vt) corresponds to a low frequency oscillation.

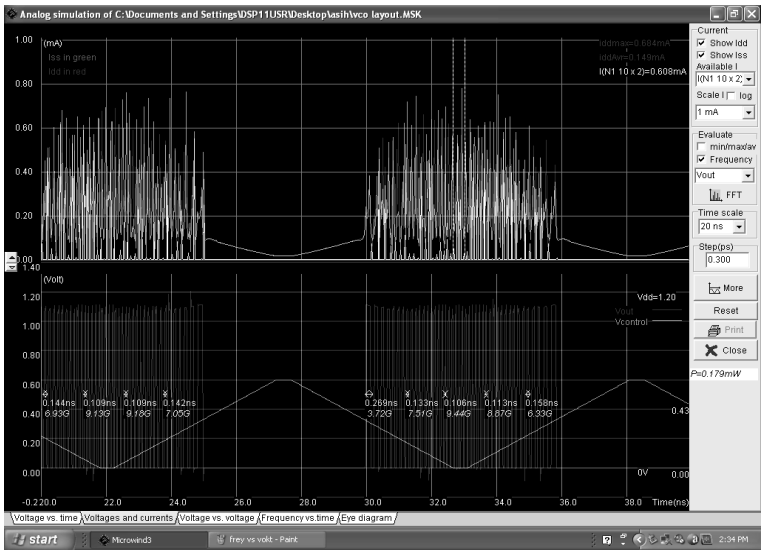

Figure7. The layout simulation of a high performance VCO circuit, voltage verses current

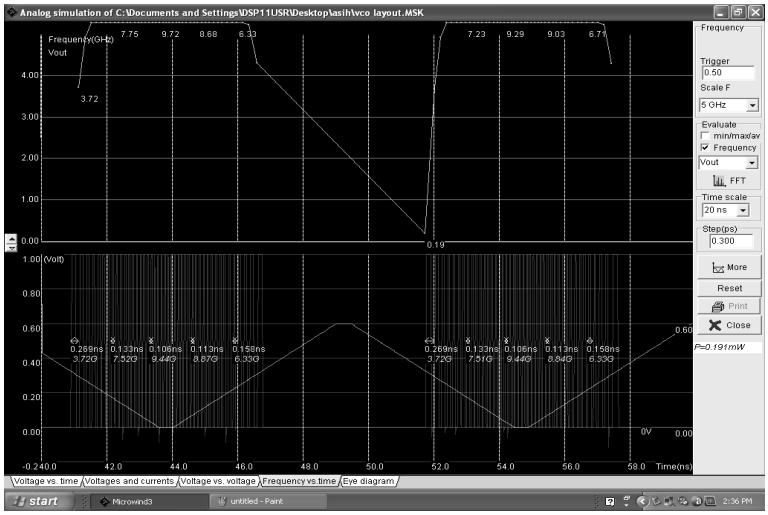

Figure 8. The layout simulation of a high performance VCO circuit, voltage verses voltage

The main drawback of this type of oscillator is the great influence of temperature and VDD supply on the stability of the oscillation. If we change the temperature, the device current changes, and consequently the oscillation frequency are modified. Such oscillators are rarely used for high stability frequency generators.

5. CONCLUSION

The Software used in paper allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

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Short Biography

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