

NEW ANALYTICAL MODEL AND SIMULATION OF INTRINSIC STRESS IN SILICON GERMANIUM FOR 3D NANO PMOSFETs

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ABSTRACT

We are proposing a new analytical model, in three dimensions, to calculate intrinsic stress that builds during deposition of Silicon Germanium pockets in source and drain of strained nano PMOSFETs. This model has the advantage of accurately incorporating the effects of the Germanium mole fraction and the crystal orientation. This intrinsic stress is used to calculate the extrinsic stress distribution in the channel after deposition. Simulation results of channel stress based on this model will be presented and discussed for Intel technology based nano PMOS transistors.

KEYWORDS

New Analytical Model in 3D, Intrinsic Stress, Silicon Germanium, Intel Nano PMOSFETs

1. INTRODUCTION

The originality of this paper is the development of new analytical model, in three dimensions (3D), to calculate accurately the intrinsic stress in Silicon Germanium ($\text{Si}(1-x)\text{Ge}(x)$) due to lattice mismatch between $\text{Si}(1-x)\text{Ge}(x)$ and Silicon where x represents the Germanium mole fraction. This intrinsic stress is generated during deposition of $\text{Si}(1-x)\text{Ge}(x)$ pockets in source and drain of Intel nano PMOSFETs (Ghani 2003). In the literature, there are only few papers and only in two dimensions (2D) about the modelling of intrinsic stress in SiGe [1]; [2]; [3]; [4]. These papers were developed in the context of device simulations for mobility modelling under the effects of stress. On the other hand, in most advanced commercial or non commercial process simulators as FLOOPS, Sentaurus, or Athena, the intrinsic stress is a user defined input. And, it is not calculated internally by the simulator.

In this paper, we are attempting to extend the 2D models found in the literature to 3D in the context of process simulation.

We are following the 2D model of Van de Walle [2]. Most of nano semiconductor device manufacturers as Intel, IBM and TSMC are intentionally using this intrinsic stress to produce uniaxial extrinsic stress in the Silicon channel.

And, it is now admitted that the channel stress enhances carrier mobilities for both nano PMOS and NMOS transistors by up to 30% [5].

Channel stress helped reduce power consumption, and increase speed of the new generation of Silicon Integrated Circuit (IC) Technology [6];[7];[8]. The electrical measurement reported for typical NMOS and PMOS nano devices show that channel stress enhanced performance of both NMOS and PMOS by up to 30% [5].

The need of the hour is the development of accurate physics based models and the use of TCAD simulation tools to understand the physics of intrinsic and extrinsic stress and how to attain the desired stress in the channel. Modelling and simulation can also explain complex stress phenomena.

This paper is organized as follows. Section 2 outlines the different sources of intrinsic stress in Si(1-x)Ge(x) pockets generated during deposition.

Section 3 describes the proposed 3D model to calculate accurately the intrinsic stress due to lattice mismatch between Si(1-x)Ge(x) and Silicon at horizontal interface in x and z directions and at vertical interface in y direction

Different extrapolation methods to calculate strained lattice constants of Silicon and Si(1-x)Ge(x) will be presented.

After deposition process, intrinsic stress produces an extrinsic stress distribution in the whole device. This section, also outlines the 3D elastic model for the extrinsic stress and how it is related to the intrinsic stress.

Section 4 presents 3D simulation results and analysis of extrinsic stress distribution in 45 nm Intel strained PMOSFETs [6] using the proposed intrinsic model. This section will also present 3D numerical results showing the effects of Germanium (Ge) mole fractions and crystal orientations on the intrinsic stress.

For qualitative and quantitative validations, the channel extrinsic stress profiles will be calculated using the proposed 3D intrinsic stress model and will be compared with channel stress profiles found in the literature.

At this point, we could not find any experimental values of intrinsic stress in 3D. Therefore, we could not provide any comparisons with experiments.

Section 5 presents the concluding thoughts and future work.

2. SOURCES OF INTRINSIC STRESS IN SIGE

The deposition process plays a key role in determining the intrinsic stress in Si(1-x)Ge(x) films. At first, we should note that the deposition takes place at elevated temperatures. When the temperature is decreased, the volumes of the grains of Si(1-x)Ge(x) film shrink and the stresses in the material increase. The stress gradient and the average stress in the Si(1-x)Ge(x) film depend mainly on the Silicon-Germanium ratio, the substrate temperature and orientation, and the deposition technique which is usually LPCVD (low pressure chemical vapour deposition) or PECVD (plasma enhanced chemical vapour deposition).

It was observed that the average stress becomes more compressive, if the Ge concentration decreases [9]. Thus, it is expected that a film with higher Ge concentration has a higher degree of crystallinity and larger grains, which leads to higher film density and to higher intrinsic stress. The intrinsic stress observed in thin films has generally the following main sources.

2.1. Intrinsic Stress Due to Lattice Mismatch

Standard During deposition, thin films are either stretched or compressed to fit the substrate on which they are deposited. After deposition, the film wants to be smaller if it was stretched earlier,

thus creating tensile intrinsic stress. And similarly, it creates a compressive intrinsic stress if it was compressed during deposition. In this paper, we are focusing on developing an analytical model in 3D for this type of intrinsic stress.

The intrinsic stress generated due to this phenomenon can be quantified by Shoney's equation by relating the stress to the substrate curvature.

2.2. Intrinsic Stress Due to Thermal Mismatch

Thermal mismatch stress occurs when two materials with different coefficients of thermal expansion are heated and expand or contract at different rates. During thermal processing, thin film materials like Si(1-x)Ge(x), Poly-silicon, Silicon Dioxide, or Silicon Nitride expand and contract at different rates compared to the Silicon substrate according to their thermal expansion coefficients. This creates an intrinsic strain and stress in the film and also in the substrate. The thermal expansion coefficient is defined as the rate of change of strain with temperature.

2.3. Intrinsic Stress Due to Doping

Author Boron doping in p-channel source/drain regions introduces a local tensile strain in the substrate due to its size mismatch with Silicon. Boron (B) atom is smaller in size than Silicon atom and when it occupies a substitutional lattice site, a local lattice contraction occurs because the bond length for Si-B is shorter than for Si-Si [10];[11].

It was reported in [11] that a single boron atom exerts 0.0141 Angstrom lattice contraction per atomic percentage of boron in Silicon at room temperature. The stress induced in the channel due to boron doping was insignificant for long-channel devices. But, for nanoscale CMOS transistors where the channel lengths are in the nanometre realm, this stress plays a significant role in determining the carrier mobility enhancement.

This tensile stress can be deleterious to the compressive stress intentionally induced by embedded Si(1-x)Ge(x) in source and drain and can result in carrier mobility much lower than expected. Also, the boron solubility in Silicon Germanium increases much beyond its limit in Silicon. So the doping stress generation problem proves to be even more significant in advanced CMOS devices where Germanium concentration is expected to be close to 30%..

Methods to counter and suppress the doping induced stress are very important issues and are still under ongoing research.

3. PROPOSED 3D ANALYTICAL MODEL

In this section, we are going to describe the proposed analytical model in 3D to calculate the three normal components σ_0^{xx} , σ_0^{yy} , σ_0^{zz} of the intrinsic stress in Si(1-x)Ge(x) due to lattice mismatch at the interfaces between Silicon and Silicon Germanium. The other three shear components σ_0^{xy} , σ_0^{yz} , σ_0^{xz} are taken to be zero.

We did follow a strategy similar to one used in the 2D model of Van de Walle [2]. We first calculate the strained lattice constants parallel and perpendicular to the interfaces in x, y and z directions. Then, from these lattice constants, we calculate the strain parallel and perpendicular to the interfaces in x, y and z directions. And, finally, we get the 3 normal stress components in 3D from the calculated strain using a modified Hookes's law. The restriction of the proposed 3D

model to 2D gives exactly the 2D model of Van de Walle. And, this is a great advantage for validations of our 3D model in 2D and its comparison to the 2D model of Van de Walle.

In 3D PMOSFET with SiGe source and drain as shown in the Figure 2, there are two interfaces between Si and SiGe: a vertical interface and a horizontal interface. In the Figure 2, the vertical interface is defined in the yz-plane and the horizontal interface is defined in the xz-plane. Let's assume that Si(1-x)Ge(x) pocket grown in source or drain area has thickness $D(\text{SiGe},h)$ and $D(\text{SiGe},v)$ at horizontal and vertical interface respectively. Let $D(\text{Si},h)$ and $D(\text{Si},v)$ be the thickness of the Silicon substrate at horizontal and vertical interface respectively. Strains will be generated due to lattice mismatch of the lattice constants. Let $A(\text{Si})$ and $A(\text{SiGe})$ be the lattice constants of unstrained Silicon and Si(1-x)Ge(x). Let $A(\text{par},h,x,i)$, $A(\text{par},h,z,i)$ and $A(\text{par},v,y,i)$ be the strained lattice constants parallel to the horizontal interface in x and z directions and parallel to vertical interface in y direction. The index i represents the Silicon or Silicon Germanium materials.

Let $A(\text{perp},h,x,i)$, $A(\text{perp},h,z,i)$, and $A(\text{perp},v,y,i)$ be the strained lattice constants perpendicular to the horizontal interfaces in x and z directions and perpendicular to the vertical interface in y direction.

We assume that there is a perfect match of the atoms of the same material at the interfaces $z=0$ and $z=z_{\text{max}}$ where z_{max} is the maximum length of the device. Then, $A(\text{perp},h,x,i) = A(\text{perp},h,z,i)$. You should see Figure 1 to have an idea about the lattice constants parallel and perpendicular to a given interface between Silicon and Silicon Germanium.

In 2D, Van de Walle assumed that $A(\text{par},h,x,\text{Si}) = A(\text{par},h,x,\text{SiGe})$ and $A(\text{par},v,y,\text{Si}) = A(\text{par},v,y,\text{SiGe})$.

In 3D, we are assuming that $A(\text{par},h,z,\text{Si}) = A(\text{par},h,z,\text{SiGe})$. For simplicity, let's assume that $A(\text{par},x) = A(\text{par},h,x,i)$, $A(\text{par},z) = A(\text{par},h,z,i)$, and $A(\text{par},y) = A(\text{par},v,y,i)$. Here i represents the materials Silicon or Silicon Germanium.

The 2D model of Van de Walle gave expressions to calculate the strained lattice constants parallel and perpendicular to the interfaces in x, y directions.

For the interface in z direction, we propose the following expressions given by:

$$A(\text{par},z) = \frac{[A(\text{Si})G(\text{Si},z)D(\text{Si},h) + A(\text{SiGe})G(\text{SiGe},z)D(\text{SiGe},h)]}{[G(\text{Si},z)D(\text{Si},h) + G(\text{SiGe},z)D(\text{SiGe},h)]}$$

$A(\text{perp},h,z,i) = A(i) [1 - D(z,i) ((A(\text{par},z) / A(i)) - 1)]$.
 The shear modulus $G(i,z)$ where i represents Silicon or SiGe materials depend on the elastic constants of the materials Si and SiGe and also depend on the orientation of interface in z direction. It is given by:

$$G(i, z) = \frac{2(C(11,i) + 2 C(12,i)) (1 - D(i, z)/ 2) }{2}$$

In this paper, the constant $D(i, z)$ depend on the elastic constants $C(11,i)$, $C(12,i)$, $C(44,i)$ of each material i. And, they also depend on the interfaces's orientations that are (001), (110), or (111). In this work, the elastic constants $C(11)$, $C(12)$, $C(44)$ for Si(1-x)Ge(x) depend on the Germanium mole fraction x and on the elastic constants $C(11)$, $C(12)$, and $C(44)$ of Silicon and Germanium that we get from Table I of Van De Walle [2].

We are going to use a nonlinear extrapolation method of Rieger and Vogl [9] to calculate C(11), C(12), and C(44) for Si(1-x)Ge(x). We calculate the constant D(i,z) that depends on the orientation of the interface in z direction by following the 2D model of Fischetti and Laux [3], and Van De Walle and Martin [2]:

$$\begin{aligned} D(i,z,001) &= 2C(12,i) / C_{-}(11,i) \\ D(i,z,110) &= [C_{-}(11,i) + 3 C_{-}(12,i) - 2 C(44,i)] / [C(11,i) + C_{-}(12,i) + 2 C(44,i)] \\ D(i,z,111) &= [C(11,i) + 3 C(12,i) - 2 C(44,i)] / [C(11,i) + C(12,i) + C(44,i)]. \end{aligned}$$

The ratio of strained lattice constants A(par,x), A(par,y), A(par,z) and A(perp,h,x,i),

A(perp,v,y,i), and A(perp,h,z,i) to unstrained lattice constants A(i) determines the intrinsic strain parallel and perpendicular to the interfaces in x, y, and z directions:

($\mathcal{E}_{par,h,x}$, $\mathcal{E}_{perp,h,x}$, $\mathcal{E}_{par,v,y}$, $\mathcal{E}_{perp,v,y}$, $\mathcal{E}_{par,h,z}$, $\mathcal{E}_{perp,h,z}$). The index i represents the material Si or SiGe. At horizontal interfaces in x and z directions, and at vertical interface in y direction, we have:

$$\begin{aligned} \mathcal{E}_{par,h,x} &= \frac{A(par,x)}{A(SiGe) - 1} \\ \mathcal{E}_{perp,h,x} &= \frac{A(perp,h,x,SiGe)}{A(SiGe) - 1} \\ \mathcal{E}_{par,h,z} &= \frac{A(par,z)}{A(SiGe) - 1} \\ \mathcal{E}_{perp,h,z} &= \frac{A(perp,h,z,SiGe)}{A(SiGe) - 1} \\ \mathcal{E}_{par,v,y} &= \frac{A(par,y)}{A(SiGe) - 1} \\ \mathcal{E}_{perp,v,y} &= \frac{A(perp,v,y,SiGe)}{A(SiGe) - 1} \end{aligned}$$

Let $\sigma_0^{xx,h,x}$, $\sigma_0^{zz,h,z}$, $\sigma_0^{xx,v,y}$, and $\sigma_0^{yy,v,y}$ be the intrinsic stress at the horizontal interface in x and z directions and at the vertical interface in y direction respectively.

We use a modified Hooke's law and similar ideas of those used in 2D model of Van de Walle to get these intrinsic stress components from the intrinsic strains as follows:

$$\begin{aligned} \sigma_0^{xx,h,x} &= (C(11) + C(12))\mathcal{E}_{par,h,x} + C(12)(\mathcal{E}_{perp,h,x} + \mathcal{E}_{par,h,z}) \\ \sigma_0^{zz,h,z} &= (C(11) + C(12))\mathcal{E}_{par,h,z} + C(12)(\mathcal{E}_{perp,h,z} + \mathcal{E}_{par,h,x}) \\ \sigma_0^{yy,v,y} &= (C(11) + C(12))\mathcal{E}_{par,v,y} + C(12)(\mathcal{E}_{perp,v,y} + \mathcal{E}_{par,h,z}) \\ \sigma_0^{xx,v,y} &= E \mathcal{E}_{perp,v,y} \end{aligned}$$

The elastic constants C(11), C(12) and the Young's modulus E are those of Si(1-x)Ge(x).

Finally, the normal intrinsic stress components σ_0^{xx} , σ_0^{yy} and σ_0^{zz} in Si(1-x)Ge(x) in the proposed 3D model are calculated as follows:

$$\sigma_0^{xx} = \sigma_0^{xx,h,x} - \sigma_0^{xx,v,y} ,$$

$$\sigma_0^{yy} = \sigma_0^{yy,v,y} ,$$

$$\sigma_0^{zz} = \sigma_0^{zz,h,z} .$$

We should note that the proposed 3D model given by the equations above reduces to 2D model of Van de Walle if we take $\sigma_0^{zz,h,z} = 0$ and $\epsilon_{par,h,z} = 0$.

The 3 shear intrinsic stress components σ_0^{xy} , σ_0^{yz} , and σ_0^{zx} are taken to be zero.

Then, the 6 components of the intrinsic stress tensor σ_0 in Si(1-x)Ge(x) are given by: $\sigma_0 = (\sigma_0^{xx}, \sigma_0^{yy}, \sigma_0^{zz}, 0, 0, 0)$.

In our simulation program, the intrinsic stress tensor σ_0 is used as a source term to calculate, in the whole 3D nano MOSFET structure, the extrinsic stress tensor $\sigma = (\sigma^{xx}, \sigma^{yy}, \sigma^{zz}, \sigma^{xy}, \sigma^{yz}, \sigma^{zx})$. We note that σ^{xx} , σ^{yy} , and σ^{zz} represent the extrinsic stress along the channel, vertical to the channel, and across the channel. This channel stress is used to enhance the mobility of holes in 3D nano PMOSFETs based on Intel technology [6]. We assume that Silicon and Silicon Germanium are elastic materials. And, to calculate the stress tensor σ , we use the elastic stress model based on Newton's second law of motion, and the following Hooke's law relating stress to strain: $\sigma = D(\epsilon - \epsilon_0) + \sigma_0$. Here D is the tensor of elastic constants C(11), C(12), C(44), $\epsilon_0 = 0$ is the intrinsic strain and σ_0 is the intrinsic stress given by the proposed 3D model. A detailed description of this elastic model is given in [12].

4. 3D NUMERICAL RESULTS AND ANALYSIS

The proposed 3D analytical model for intrinsic stress is used to simulate numerically the 3D extrinsic stress in the channel of an Intel 45 nm gate length PMOSFET shown in Figure 2. For the following numerical results we used (001) for the substrate orientation and 17% as the Germanium mole fraction. In the future, we will do more investigations using different gate lengths (32nm, 22nm and below), different substrate orientations and Germanium mole fractions. The Table 1 shows the effects of Germanium mole fraction on the intrinsic stress in Si(1-x)Ge(x).

From Table 1, we observe that the intrinsic stress along channel in x direction becomes more compressive, if the Ge concentration increases. This is in great agreement with what was reported in [5]. Table 2 shows the effects of substrate orientations on the intrinsic stress.

The results in Figures 3 and 4 show that the stress components σ^{xx} and σ^{zz} along the channel, and across the channel respectively are all significant. This is an important finding of

this paper. A similar stress distribution has been reported in [13]. The values of the calculated 3D extrinsic stress are also qualitatively and quantitatively in good agreement with those calculated in [13]. Figure 5 shows that the distribution of x stress component is compressive along channel as expected. Figure 6 shows that the distribution of the z stress component is really non-uniform in the channel. A similar result was reported in [13]. These numerical results confirm that our implementation of intrinsic and extrinsic stress models in 3D provide valid and correct results. We also believe that these results are of great interest to the semiconductor community including industrials and academia.

Ge %	σ_0^{xx}	σ_0^{yy}	σ_0^{zz}
17	-1.432e+10	3.269e+9	1.752e+9
20	-1.674e+10	3.821e+9	2.047e+9
30	-2.454e+10	5.607e+9	3.914e+9
40	-3.197e+10	7.312e+9	3.914e+9
50	-3.900e+10	9.321e+9	4.780e+9

Table 1: Effects of Germanium mole fraction on intrinsic stress

Orientation	σ_0^{xx}	σ_0^{yy}	σ_0^{zz}
(100)	-8.859e+9	1.186e+10	6.361e+9
(110)	-1.432e+10	3.269e+9	1.752e+9
(111)	-1.556e+10	1.327e+9	7.116e+8

Table 2, Effects of substrate orientation on intrinsic stress

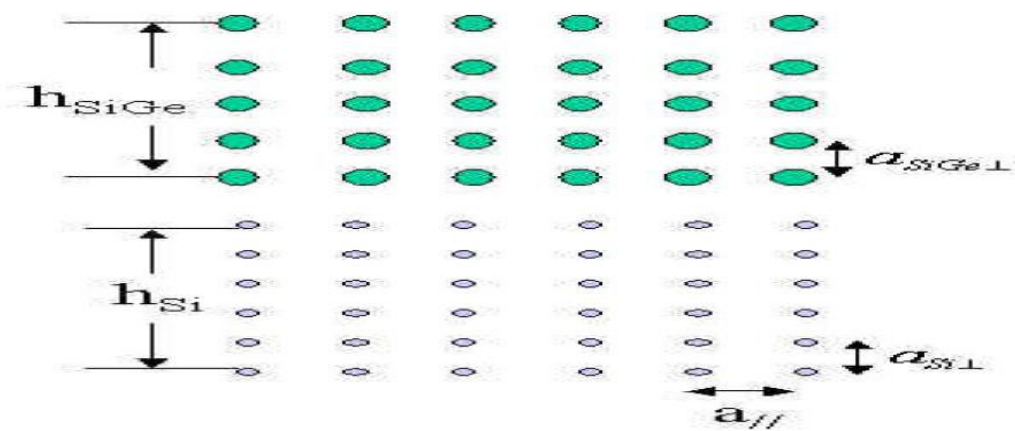


Figure 1, Lattice constants parallel and perpendicular to the interfaces

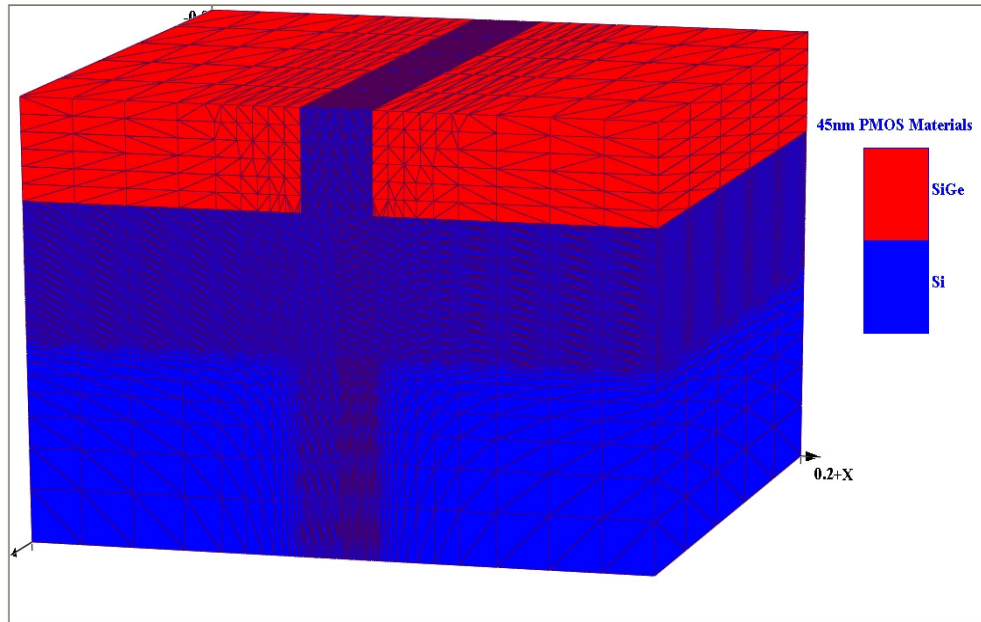


Figure 2, Materials and mesh of the simulated structure

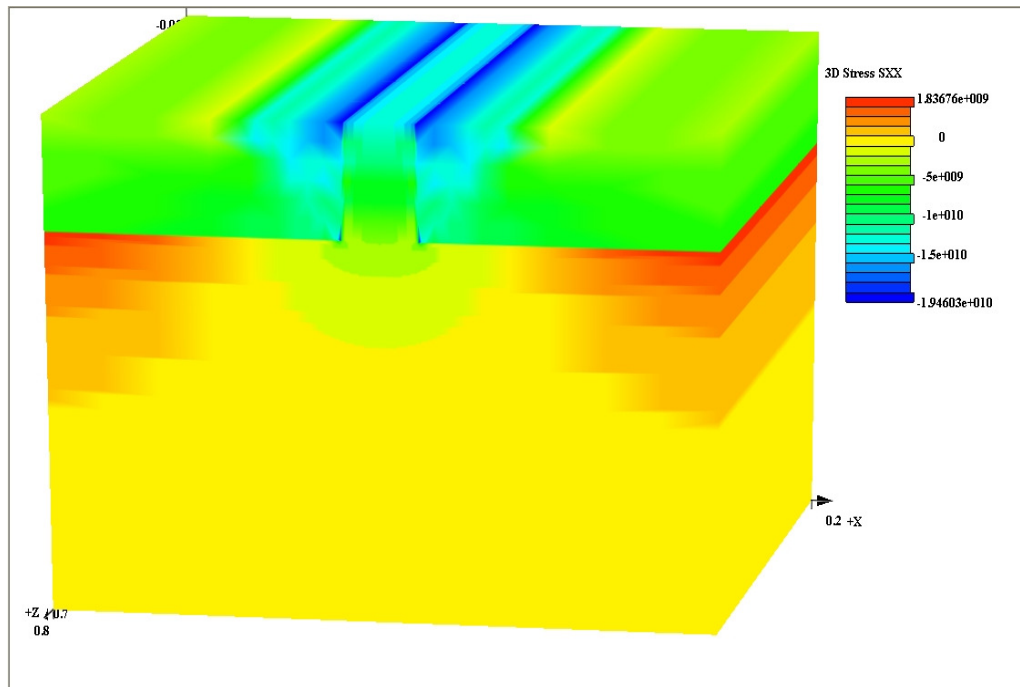


Figure 3, 3D distribution of x stress component along channel

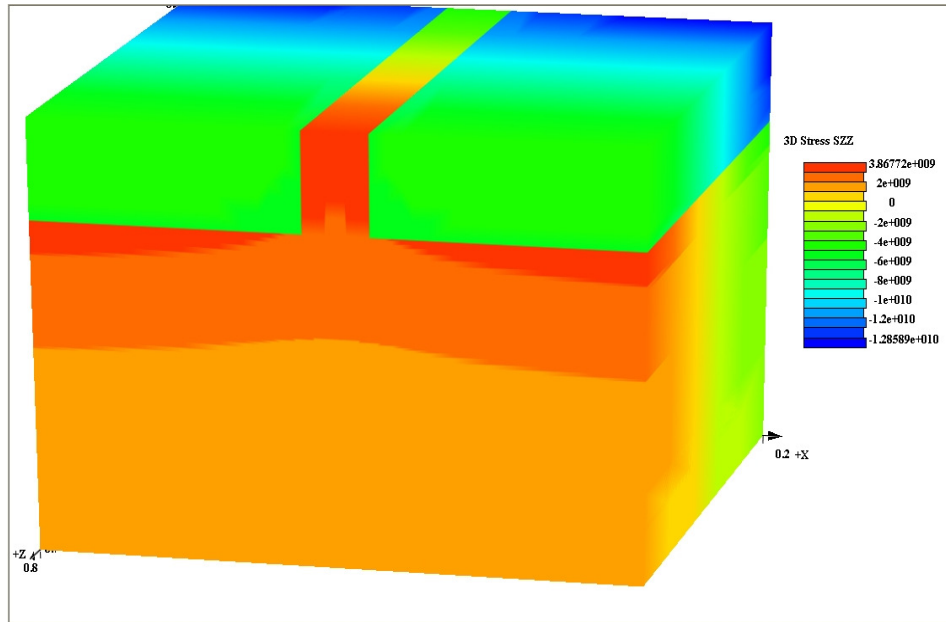


Figure 4, 3D distribution of z stress component across channel

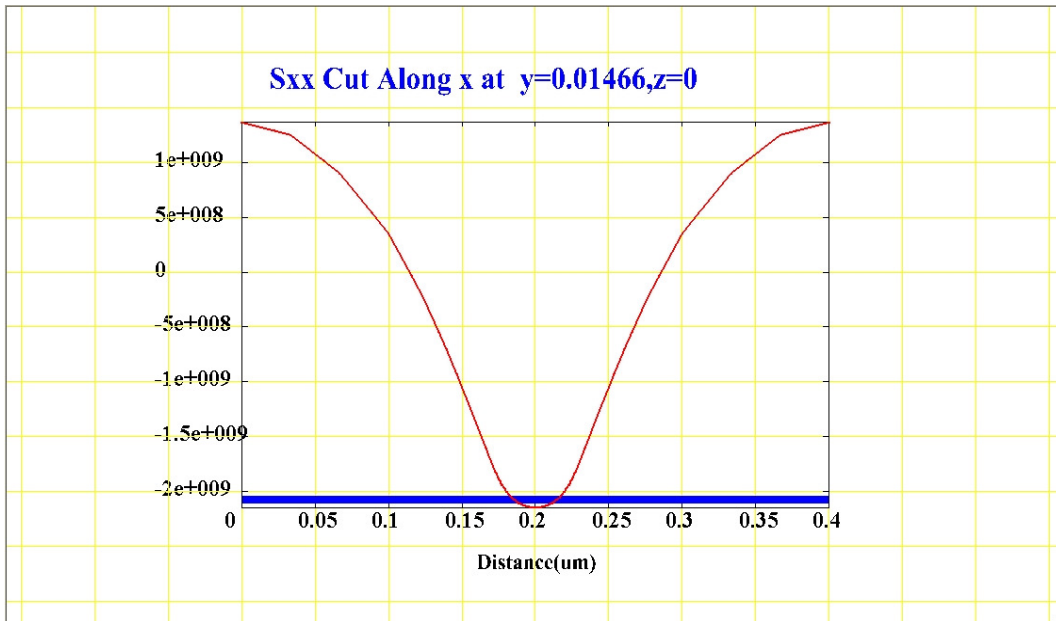


Figure 5, Cut along channel in x direction of x stress component



Figure 6, Cut across channel in z direction of z stress component

5. CONCLUSIONS

In this paper, we have developed a new analytical model in 3D to calculate the intrinsic stress that builds during deposition of Silicon Germanium pockets in source and drain of a strained nanometre PMOSFETs. This model has been implemented and used successfully to simulate the extrinsic stress in the channel of an Intel 45 nm gate length PMOSFET shown in Figure 1. The important finding of this paper is that all the stress components σ^{xx} and σ^{zz} along the channel, and across the channel respectively are significant. On the other hand, this paper did show that the distribution of the z stress component is really non-uniform in the channel. The quantitative and qualitative behavior of the numerical results is in good agreement with those found in literature [13] for similar 3D structure.

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