

FIELD PROGRAMMABLE GATE ARRAY BASED CONTROL SIGNAL GENERATOR FOR PULSED RADAR

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ABSTRACT

The objective of this paper is to present the architecture design and implementation of a software defined hardware module called Control Signal Generator (CSG) for pulsed RADAR (Radio Detection and Ranging) application. It is a digital, programmable, application-specific control timing signal generator for Disaster Management Synthetic Aperture Radar (DM-SAR)[1]. This module is a slave controller which receives command through asynchronous serial interface and generates programmable timings. Architecture evolved and the module is developed using Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL)[2] and successfully implemented on Xilinx Field Programmable Gate Array (FPGA) XCV600-6HQ240 [3].

Keywords

Field Programmable Gate Array, VHDL, RADAR, Control Signal Generator, TSG, PRI.

1. INTRODUCTION

The Synthetic Aperture Radar (SAR) is pulsed radar for on-demand imaging under all-weather conditions for a variety of purposes and the DM-SAR project is aimed at realizing a flexible and configurable product for use in disaster management applications. The central controller of the radar unit called the Radar Controller is the control-center of the system and sports a microcontroller along with hardware resources. It performs all system setup, command, control applications and also provides user interface through a serial link to an operator console.

The fast-advancing area of software defined hardware enabled by the exponential development per-device resources in field-programmable gate array (FPGA) technology has made inroads into most electronic design environments. The developmental flexibility and the level of design automation possible with these devices have made the use of FPGAs very convenient and productive. Complex radar control electronics is no exception; in fact it is a great beneficiary of the advantages offered by FPGAs [4] in realizing complex timing and logical interlocks often required in such systems.

This paper describes architecture and the design implementation of a module for generating certain specific control signals using the FPGA in the radar controller of the radar unit. This application-specific architecture and module reduces resource-demand significantly compared to standard component's IP cores (IP of commercially of the self available components like 8054 timer) as well as Processor based system for executing similar functions. Independent modules running in parallel can provide substantial savings in sequential software overheads of Processor based system.

2. REQUIREMENTS

There are three basic operational control signals: 1. Transmit (Tx) Pulse, 2. Transmit (Tx) control and 3. Receive (Rx) Data Window. Tx pulse marks the duration of transmission of a waveform-coded, pulse-modulated 5.35Ghz signal. In this window, Radio Frequency (RF) subsystem generates linear-frequency modulated "chirp" signal which is amplified by Travelling Wave Tube Amplifier (TWTA) prior to transmission. Tx Control is an extended TX pulse having front and back porch extensions to take care of rise time requirements of the TWTA as well as to protect receiver by removing receiver input through a switch during this period. These signal repeats at Pulse Repetitive Interval (PRI) rate.

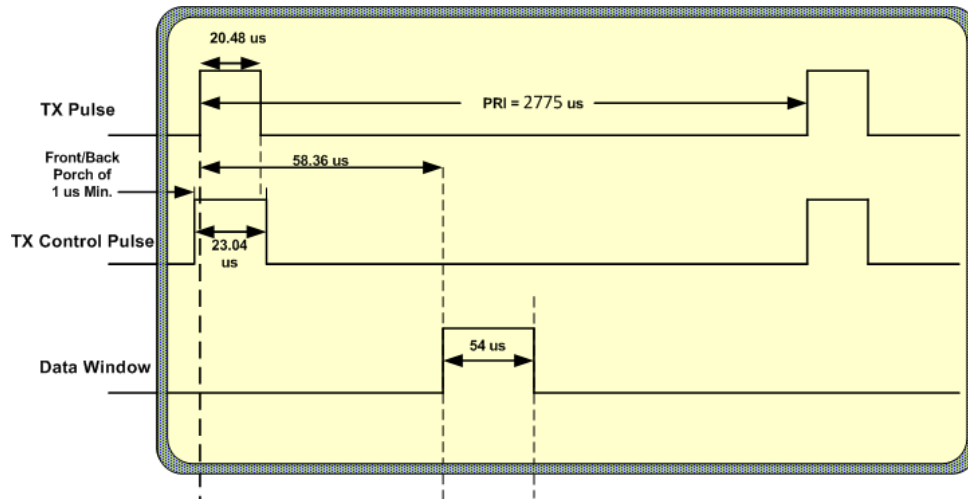


Figure 1. Control Timings

Figure 1 shows typical requirements for eight kilometer height and 80° look angle of antenna [4]. Signal generation accuracy should be within 256 nanoseconds. All signals should be programmable and synchronized with system clock.

3. DESIGN SOLUTION

The Control Signal Generator (CSG) has been designed using modular approach, and consists of three basic modules: 1. Command Decoder, 2. Local Bus and 3. Timing Signal Generators, This architecture is similar to a standard microprocessor based system [5].

Figure. 2 show architecture for CSG application. Command Decoder interfaces with external full duplex asynchronous serial link and generates signals for the internal local bus. The internal local bus provides interface among the modules. There are four Timing signal generator (TSG)

modules to generate three control signals and fourth one to generate synchronization pulse (sync) at rate of Pulse Repetitive Interval. Delay period (Logic level low) and On Pulse Width (High Logic Level) of each control signal is programmable and generates with reference to internally generated sync signal.

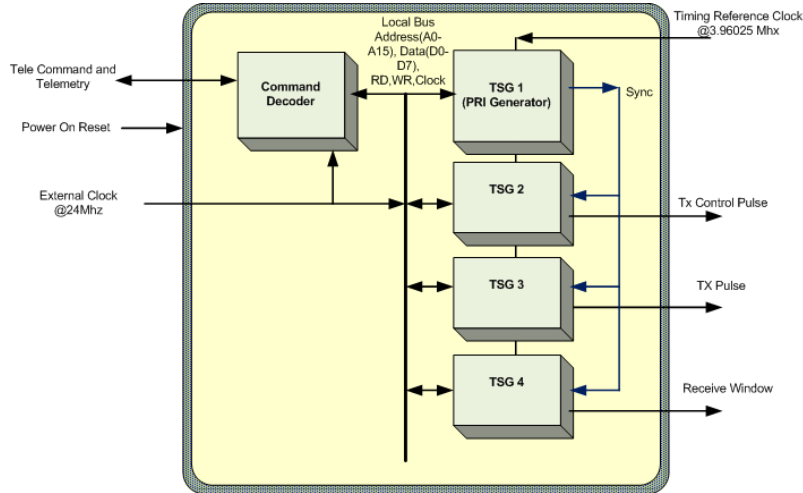


Figure 2 .CSG Architecture Block Diagram

CSG operates on two clocks. External clock 24 Mhz is basic clock on which internal logic works. This clock is six times higher than timing generation requirements of 256 nanoseconds. Power On Reset signal generates logical reset to internal logic. Three control signals are generated using counters inside TSG running on external timing reference clock of 3.90625 MHz with programmable resolution of 256 nanoseconds which meets resolution requirement.

3.1 Command Decoder

The command decoder consists of three dedicated modules including: Universal Asynchronous Receiver Transmitter (UART), UART Controller and Command Decoder. This block as a whole realizes embedded controller interface within an FPGA which interfaces with the outside world through RS-232 serial communication link, receives & decodes specific commands and generates a standard microprocessor control interface consisting of 16-bit address bus, 8-bit data bus & control signals. Figure 3 represents block diagram of Command Decoder module.

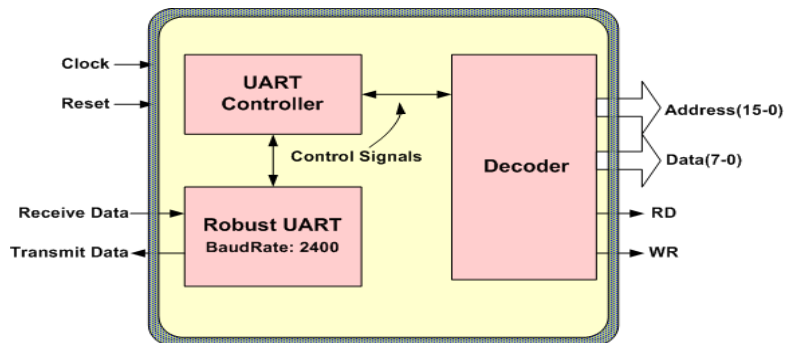


Figure 3. Command Decoder Module

The UART module is a robust interface to implement full duplex asynchronous serial communication protocol within FPGA. This UART give 6 times better performance in presence of noise in Data reception [6]. It has one input signal (Receive Data) and one output signal (Transmit Data) that operates in full duplex mode. Protocol is fixed to Baud Rate 2400, No Parity, 8 Data bits, No parity and 1 Stop bit.

The decoder module is responsible for decoding the incoming command format, converts received ASCII (American Standard Code for Information Interchange) byte into their equivalent hex digits representation and generate local bus controls comprising of word wide address bus, byte wide data bus, read and write signals. The format of command and response is in ASCII. Decoder supports two commands for write and read,

1. $WA_3A_2A_1A_0D_1D_0$: Write 8-bit data byte D_1D_0 (LS byte) into memory address $A_3A_2A_1A_0$ (LS byte). One write operation requires 29.17 milliseconds.
2. $RA_3A_2A_1A_0$: Read 8-bit data byte from memory address $A_3A_2A_1A_0$. One read command requires 20.84 milliseconds and 29.17 millisecond including data reception with negligible latency time.

UART Controller module generates required control signals for the command decoder module & maintains synchronization between UART & the command decoder module. Following Figure 4. Command decoder simulation gives ModelSim [7] simulation result of write/read command received on rxd line, read data transmitted on txd line, internal address (addr), data, write and read signals generated for addresses $4001_{(H)}$ - $4004_{(H)}$ on bus addr. Write operation performed on addresses $4001_{(H)}$ - $4004_{(H)}$ and read on $4001_{(H)}$. RxData signal is latch data because of signal wr_d1 that is internal signal for write. Same way for read operation rd signal results in to tx_data which will be transmitted serially on txd.

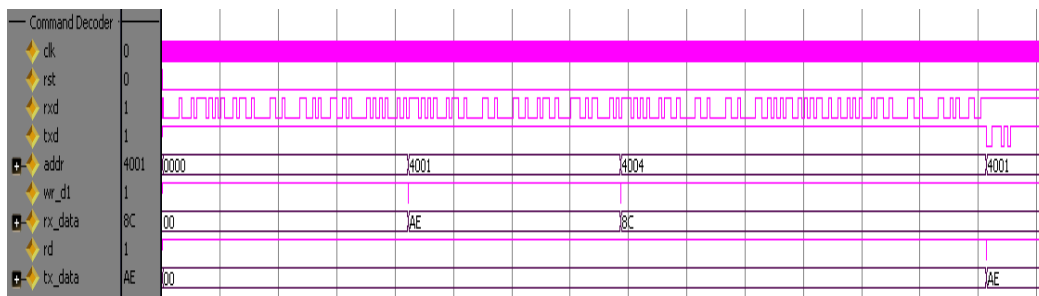


Figure 4. Command decoder simulation

3.2 Timing Signal Generator (TSG)

Timing Signals can be generated using standard timer IP [8]. Considering advantage of implementation and flexibility for specific application, Timing Signal Generator (TSG) is a module based on Unified Timing Signal Generator [9]. The UTSG is application specific timing signal generator that meets timing requirements of pulsed RADAR (Radio Detection and Ranging). It has six modes to cover different requirements. This is modified to make design compact by using first four modes. This trimmed version having resource utilisation per TSG instantiation 3.5% instead of 7% for XCV600 device is used.

3.3 Local Bus

Local bus is for interface among designed modules. Internal bus is selected byte parallel. Bit serial bus like SPI (Serial Peripheral Interface) requires additional hardware about 300 LUT(Look Up Table) logical units [10] for controller and also reduces transfer speed by 1/8 factor for a byte transfer. Basic control bus consists of sixteen bits address bus, 8 bits data bus and control signals (Write, Read) required interfacing internal modules along with 24 MHz clock signals as per Figure 4. Each module on bus has its own address decoding logic.

3.4 Configuration

Control Signal Generator is configured to generate three timing signals namely 1. Tx control pulse, 2. Tx pulse & 3. Receive window. Timing signal generator modules are configured by programming its register bank consisting of six, 8 bit registers and each separated by 32 addresses. Each parameter of OFF Time and ON time is formulated by 16 bits that gives programmability from 0 to 16.776 milliseconds having resolution of 256 nanoseconds. TSGs are assigned specific address range through which they can be programmed to operate in configured modes. Timing signal generated by the first TSG acts as an external reference signal for other TSGs as shown in Figure 2. Programmable timing signals are generated according to the configuration tabulated in Table 1.

Table 1. TSG Configuration

Sr No	TSG	Address Range	Registers Value in hex	Remarks
1	TSG1	4000h -> 401Eh	On:8 Off:2B5C	Mode 1: Free running/ Oscillator Mode Generates a reference signal at PRI rate for other TSGs
2	TSG2	4020h -> 403Eh	On:0051 Off:0008 No of pulse:0001	Mode 3: MonoShot –HW Gated Generates Tx control pulse with programmable delay & width
3	TSG3	4040h -> 405Eh	On:005C Off:0004 No of pulse:0001	Mode 3: MonoShot –HW Gated Generates Tx pulse with programmable delay & width
4	TSG4	4060h -> 407Eh	On:00D8 Off:00E9 No of pulse:0001	Mode 3: MonoShot –HW Gated Generates receive window with programmable delay & width

Configuration of TSG requires six addresses in mode1 and eight addresses in mode3. Total 30 registers updates requires for configuring four TSGs. This requires 876 milliseconds to write configuration.

4. TEST RESULTS

The Control Signal Generator (CSG) is developed on a single board Xilinx FPGA XCV600-4HQ240[3] based card with trans-receivers for electrical compatibility with external logic levels. There are four elements in total test setup as shown in Figure 5.

1. FPGA Board.
2. Multi output calibrated Programmable Power Supply from Agilent to generate +5V DC, +3.3V DC and +2.5V DC.
3. A PC running GUI based control program to send/receive command string through serial communication port (COM Port). This software is developed using Visual Basic 6 on MS-Windows XP platform.
4. Oscilloscope to measure and record the waveforms.



Figure 5. Test Setup

Functional testing of the Control Signal Generator has been carried out by creating a VHDL project with four instantiations of the TSG modules as shown in Figure 6. Instances are named as TSG1-4. CD is clock divider block inserted for simulation purpose which generated timing reference clock of 3.90625 Mhz. However for simulation purpose timing reference clock generated as 4 MHz clock from 24Mhz. In implementation the clock will be fed externally. DEC is decoder to select TSGs. ISE 10.1i [11] EDA tool is used for compilation and implementation of design.

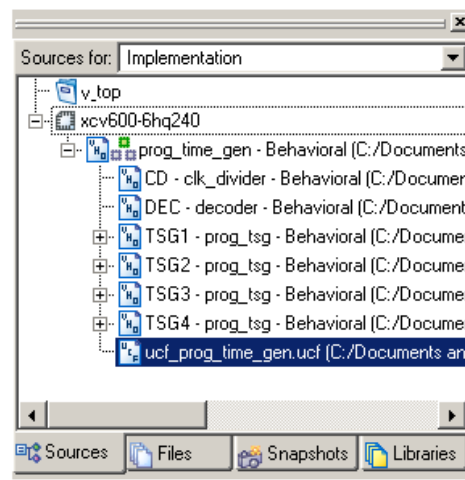


Figure 6. Implementation Project View

External input through serial link is supplied using a PC communication port. TSG registers were loaded with values as per Table 1. TSG Configuration to configure application requirements. Output timing signal was observed on oscilloscope.

RTL Simulation result of design is in Figure 7. Reference pulse (ref) signal is by TSG1. Configuration sequence is as per Table 1. For capturing of simulation result of two pulses, PRI rate is increase in simulation. TX pulse, Tx control pulse and Data windows are simulated for actual values.

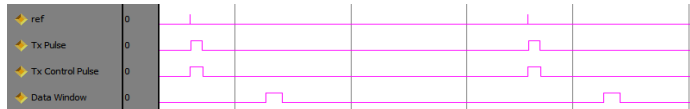


Figure 7 Simulation Result

Measured results are given in Figure 8 that measures Tx Pulse width of 20.34 microseconds and Tx control pulse of 23.05 microseconds. Signals generated are in multiples of 256 nanoseconds and its count value is programmable through commands.

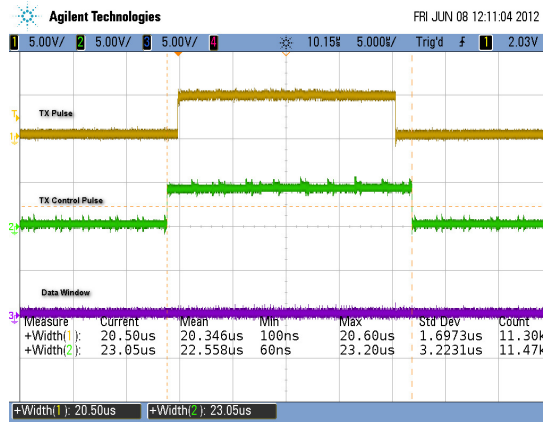


Figure 8. TxPulse Measurement

Figure 9 is measurement result of data window width that is 54.0 microseconds.

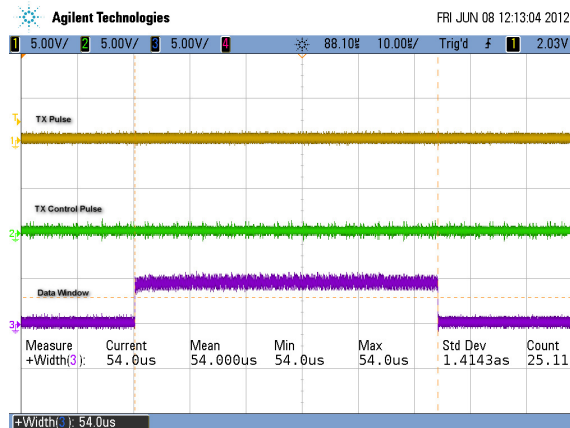


Figure 9. Data Window Measurement

Figure 10. is measurement of delay from rising edge of TX Pulse to rising edge of Data Window that is of 58.4 microseconds.

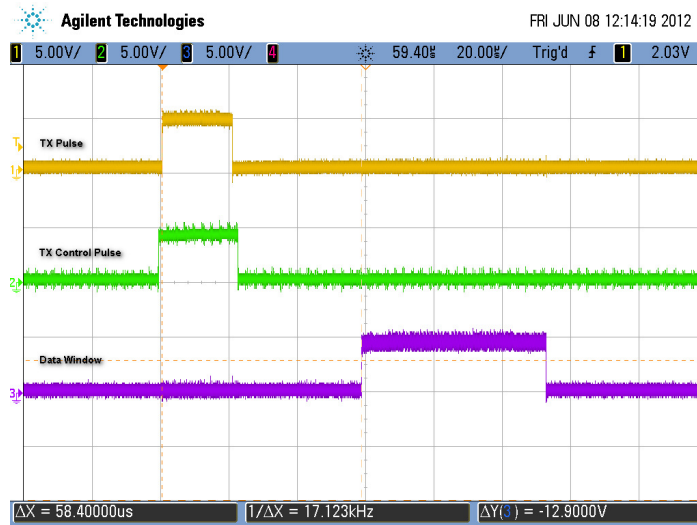


Figure 10 .TxPulse to Data Window Delay

Following Figure 11 shows repeated generation of the signals. The period of the signal is 2.77 millisecond.

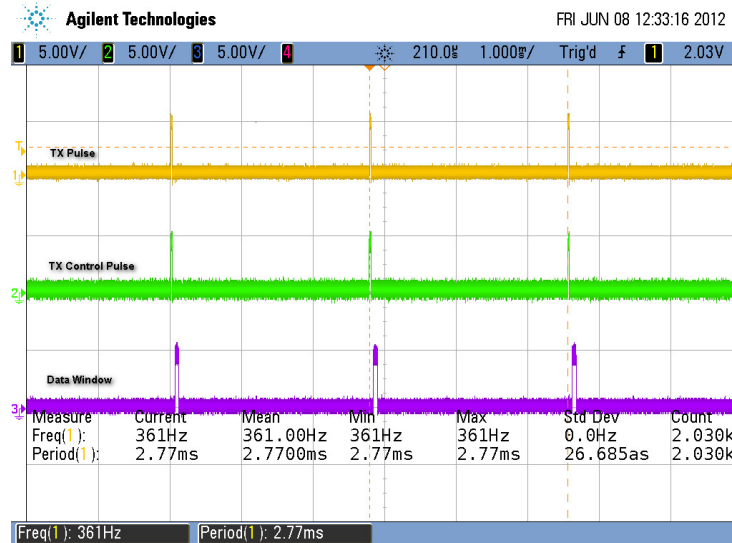


Figure 11 .PRI Measurement

5. RESOURCE UTILISATION

Table 2. Device Utilisation represents implementation result mentioning resource utilization of the device Xilinx Virtex FPGA-xcv600-6HQ240. About 20% utilization of the resources is demanded by this architecture. This gives very good margin for expansion.

Table 2. Device Utilisation

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	1517	6912	21%
Number of Slice Flip Flops	1570	13824	11%
Number of 4 input LUTs	2405	13824	17%
Number of bonded IOBs	51	166	30%
Number of GCLKs	2	4	50%

6. COST BENEFIT RATIO

Standard IP based solution requires LUT in range of 2000-6000 based on processor core[12]. Additionally external memory is required for program storage / data handling and application specific modules too. Here 2405 LUT cover total application.

7. CONCLUSIONS

A control signal generator module has been designed for the requirements specified at the outset. Post simulation, the design was ported to Xilinx -Virtex family environment devices XCV600-6HQ240 and, it has been thoroughly tested. The performance has been verified with requirements and found to be very satisfactory. All timings in the control signal generator are programmable and the design goals have been achieved.

The architecture is application specific modular and provides advantage of reusability, compactness and expandability over standard IP core or using discreet logic devices. It provides a framework for similar applications.

The module may be enhanced by future work on this lead by adding other application specific modules. Also this application uses 2400 baud serial communication commensurate with the systemic requirements (Command write time = 29ms, command read time = 20.5ms); further optimization on this count and command decoder is possible for more time-demanding applications.

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