CMOS 8-BIT BINARY TYPE CURRENT-STEERING DAC

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ABSTRACT

A CMOS 8-bit binary type current steering Digital to Analog Converter DAC with dynamic random return to zero technique to improve dynamic performance is presented in this paper. Current steering DAC has advantage of constant output impedance and high conversion rate. To demonstrate the proposed technique, 8 bit CMOS DAC is designed and layout is prepared in 90 nm technology. Computation of Integral Non Linearity (INL) and Differential Non Linearity (DNL) performance parameter is done. Chip layout consumes 57 mW power and 5483 $(\mu m)^2$ area.

KEYWORDS

Current steering, Digital-to-Analog Converter (DAC), Digital Random Return to Zero (DRRZ).

1. INTRODUCTION

In applications such as wireless communication, digital video and audio requires cost-effective data converters that can achieve higher speed or conversion rate and resolution. A wide range of digital-to-analog converter (DAC) exists, each has its own advantages. The DAC can be categorized into Binary weighted DAC, R2R ladder DAC, Segmented DAC, Current- steering DAC. Binary weighted DAC, R2R ladder DAC, Segmented DAC has disadvantages of medium conversion rate. The current-steering DACs can achieve high conversion rate and thus are used in high frequency signals. This type is called current-steering DAC since it uses current throughout the conversion as compared to other DACs where a voltage is converted into current which is then used to generate voltage at the output. Current-steering type of DACs requires precision current sources that are summed in various fashions. Current-steering DACs have one advantage of high current drive inherent in the system and, since output buffers are not required to drive resistive load this DACs are used in high speed applications. There are two types of current-steering DACs first type requires a set of current sources each of unit value of current I, i.e. for N-bit 2^N-1 current sources are required, second type is called current-steering DAC with binary weighted current sources, as the name specifies current sources are binary weighted and for N-bit N current sources of various sizes are required. The first type of current-steering DAC requires digital input in the form of thermometer code, on the other hand in second type current-sources are binary weighted thus input code can be a simple binary number. In thermometer code there will be all ones from Least Significant Bit (LSB) up to the jth bit for digital input M_j and all other bits above it are zero. It is named as thermometer code since code changes from all once to all zero resembling to a thermometer.

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Figure 1 shows the overview of current steering DAC. There are three types of current steering DACs Binary, Uniary and segmented [1]. The scheme of current cells used in these types of current steering DAC is shown in figure 1. In binary current steering scheme, four single current cells are used with value I, 2I, 4I and 8I. The advantage of binary current steering scheme are

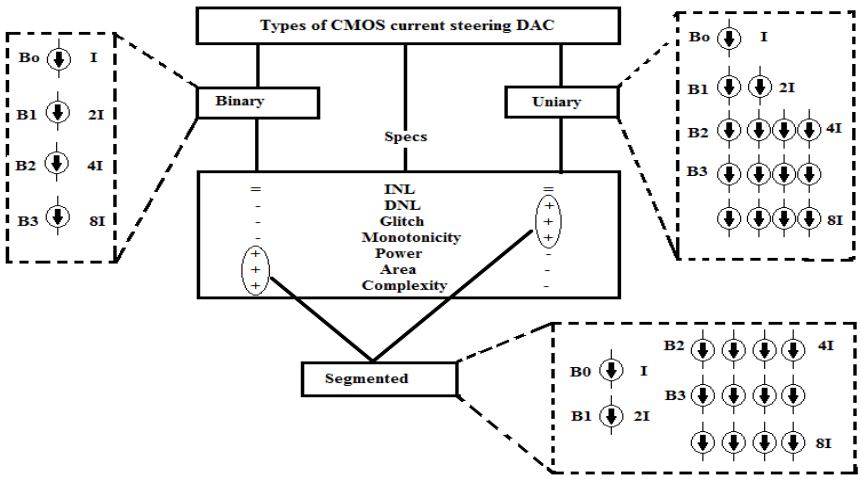

Figure 1. Overview of current steering DAC.

power consumption is less, area occupied is less and complexity of design is less. In uniary type current steering DAC, for I one current cell is used for 2I two current cells are used for 4I four current cell are used and for 8I eight current cells are used. The advantage of uniary type of current steering DAC is that its output has monotonicity, good DNL and less glitch. In segmented type of current steering DAC it has single current cell for I and 2I, four and eight current cells for 4I and 8I respectively. The advantage of segmented current steering DAC is advantage of both binary and uniay type current steering DAC.

Figure 2 shows the generic form of current-steering DAC. It consists of 2^N-*1* current cell of constant I_u output current. Each current cell consists of a clock CK driven latch, a pair of p-channel MOSFET functioning as a current switch and a constant current source. Each latch is

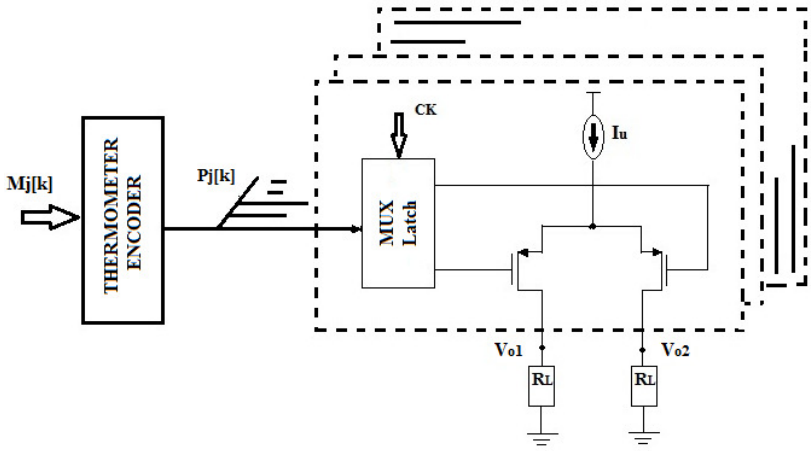

Figure 2. Generic form of current-steering DAC.

driven by CK with input from encoder. The complementary outputs of the latch drives the current switch passing the current I_u through one of the load R_L at a time. The digital input $M_i[k]$ is given to the thermometer encoder which converts it into N thermometer-code signals $E_j[k]$, where $1 \leq j \leq N$, such that $M_i[k] = \sum_{j=1}^{N} P_j[k]$. The $P_j[k]$ signal has value of either (+1) or

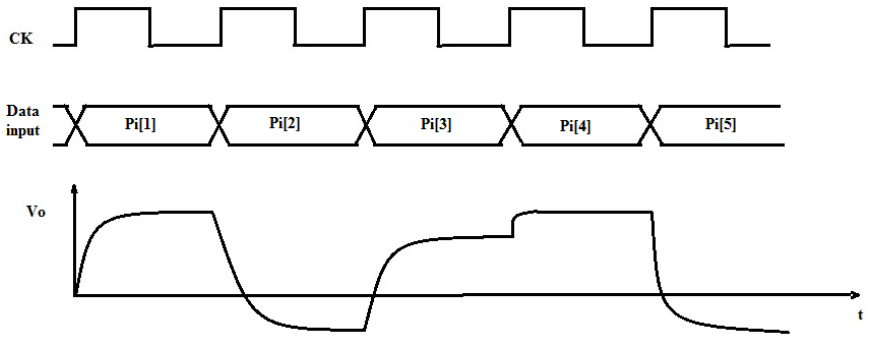

Figure 3. NRZ output waveform of a current-steering DAC.

$V_o = V_{o1} - V_{o2}$. V_o has a voltage range between $+NI_uR_L$ and $-NI_uR_L$ and a step size of $2I_uR_L$. Dynamic performance specification of DAC are expressed in terms of conversion rate and input signal frequency. DAC static linearity, specified as Integral Non-linearity (INL) and Differential Non-linearity (DNL), is determined by matching of I_u among different current cells and the output resistances of the I_u current sources. However with ideal I_u dynamic non-linearity still occurs. It is calculated as Spurious Free Dynamic Range (SFDR), which is ratio of the analog signal power to the power of the strongest distortion component within a certain frequency band. SFDR degradation is calculated in the V_o output spectrum when the $M_i[k]$ is a single tone sine wave. The SFDR decreases rapidly with increasing input frequency. The sources of dynamic non-linearity in current-steering DAC are numerous and complex, including code dependent switching transients [1], [2] and the capacitive output impedance of the current cells [3], [4], [5].

The return to zero (NRZ) technique has been proposed to improve the DAC dynamic performance [1], [9], [10]. These technique adds an buffer between output load and current switches and executes current-switching operation in the zero phase. Also DAC dynamic performance can be improved by making switching transients uncorrelated with the input sequence by modifying the current-switching operation [6], [7], [8].

In this brief, Digital Random Return to Zero (DRRZ) technique has been proposed to mitigate the effect of switching transients on the DAC performance [11]. To demonstrate the proposed technique an 8-bit 1.6 Gs/S current-steering DAC layout has been designed. The rest of this brief is organized as follows, section 2 introduces the DRRZ scheme. Section 3 shows the results and comparison. Section 4 draws conclusions.

2. DRRZ SCHEME

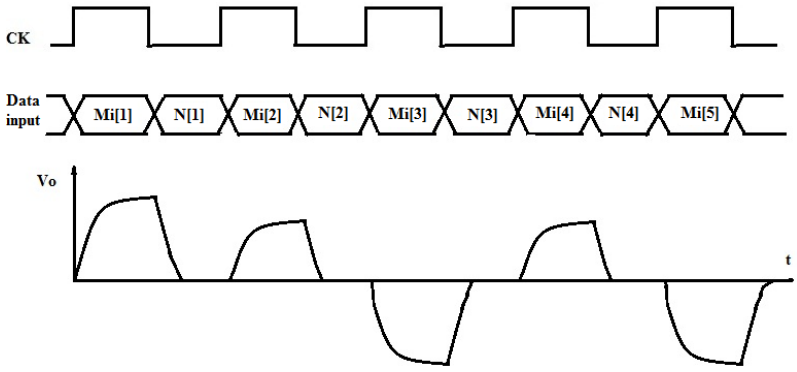

Figure 4. Waveform of RZ DAC.

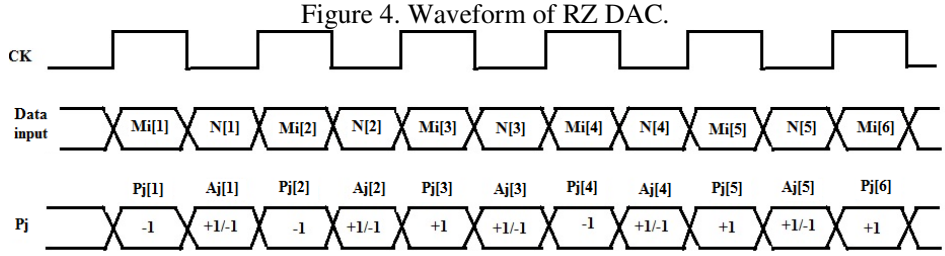

Figure 5. Switching behavior of current cell in DRZ DAC or DRRZ DAC.

Consider the *j*th current cell of the DAC shown in Figure 2. The current-switch is driven by complementary outputs from the latch corresponding to $P_j[k]$, where $P_j[k] \in \{-1,+1\}$. When CK changes from low-to-high, the current switch may remain unchanged or undergo a switching from (-1)-to-(+1) or a (+1)-to-(-1). When the current-switch makes a switching, the DAC output V_o experiences a transient disturbance called switching transients. For the Non-Return to Zero (NRZ) DAC, the switching of the current cell is controlled by the input $M_i[k]$. Thus switching transients depends on input and will result in DAC dynamic distortion.

Analog Return-to-Zero (ARZ) scheme has been used to hide the switching transients from the output [1], [9], [10]. Figure 4 shows the V_o waveform of the ARZ operation with reference to CK and input signal $M_i[k]$. When CK is high, the DAC is in the data phase and when CK is low, the DAC is in the zero phase. In the data phase analog output V_o is generated by setting up the current switches corresponding to input $M_i[k]$. In the zero phase, output V_o is forced to zero by current switches added at the output nodes V_{o1} and V_{o2}. The current switches in the DAC are switched to reflect the next input $M_i[k+1]$ during the zero phase. Thus switching transients do not appear in V_o to contribute dynamic distortion.

However, in case of Digital Return-to-Zero (DRZ) setup switching transients appear in V_o. Consider the *j*th current cell. Figure 5 illustrates the switching behavior of current cell corresponding to P_j. When CK is high, $P_j = P_j[k]$ is determined by the input $M_i[k]$. When CK is low $P_j = A_j[k]$ is a fixed value of either (+1) or (-1). In figure 5, $P_j[1] = -1$ and $P_j[2] = -1$ have the same value. If $A_j[1] = -1$ then there will be no switching transition during the $N[1]$ period. If $A_j[1] = +1$, there will be (-1)-to(+1) and (+1)-to-(-1) transients on both edges of the N[1] period. Figure 5 also shows that $P_j[2] = -1$ and $P_j[3] = +1$ have different values. If $A_j[2] = +1$, a (-1)-to-(+1) transient occur at left edge of $N[2]$ period. If $A_j[2] = -1$, a (-1)-to-(+1) transient occur at right edge of $N[2]$ period. Similarly in case of $P_j[3] = +1$ and $P_j[4] = -1$, (+1)-to-(-1) transient occurs at left edge if $A_j[3] = -1$ and (+1)-to-(-1) transient occurs at right

edge of *N[2]* period if $A_j[3]$=+1. In summary, DRZ assigns a constant to $A_j[k]$ i.e., $A_j[k]$ = +1 for all *k* or $A_j[k]$ = -1 for all *k*. Thus the current switch transitions are determined by the $P_j[k]$ sequence alone. Their strong correlation with the input $M_i[k]$ yields distortion in V_o.

The proposed DRRZ technique randomizes the switching transients appearing in DRZ. In this scheme, the switch controls $P_j[k]$ in the *N[k]* phase are dictated by a Pseudo Random Number Generator (PRNG), such that $\sum_{j=1}^{N} E_j[k] = 0$. Consider the *j*th current cell and the operation sequence shown in the figure 5. When CK is high $P_j = P_j[k]$ is determined by the input $M_i[k]$. When CK is low, $P_j = A_j[k]$ becomes a binary random variable, which has a value of either (+1) or (-1). In figure 5, $P_j[1]$=+1 and $P_j[2]$=+1 have the same value, thus switching transition occurs only if $A_j[1]$ = -1 else there will be no switching transition during the *N[1]* period. Figure 5 also shows that $P_j[2]$ = +1 and $P_j[3]$= -1 have different values. If $A_j[2]$ = -1, a (+1)-to-(-1) transient occur at left edge of *N[2]* period. If $A_j[2]$=+1, a (+1)-to-(-1) transient occur at right edge of *N[2]* period. Similarly in case of $P_j[3]$ = -1 and $P_j[4]$ = -1, (-1)-to-(+1)

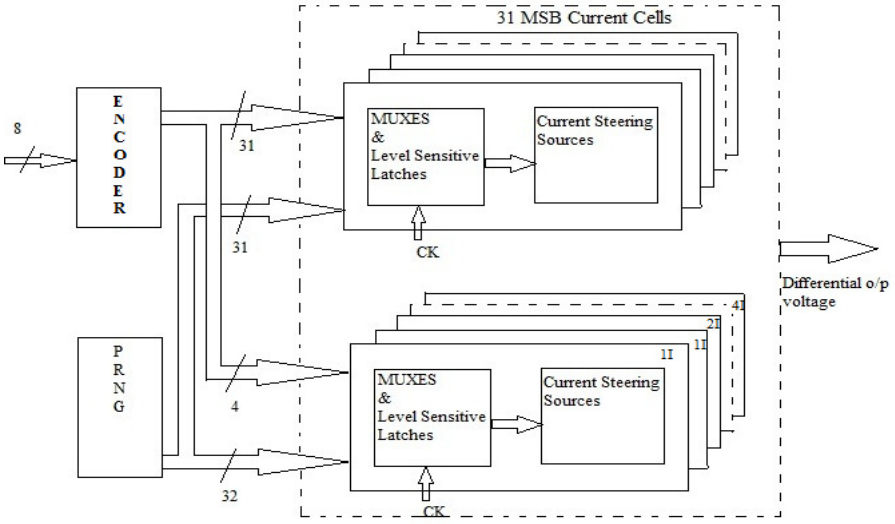

Figure 6. Block diagram of DRRZ DAC.

transient occurs at left edges and (+1)-to-(-1) transient occurs at right edge of *N[2]* period if $A_j[3]$=+1 else there will be no transient if $A_j[3]$ = -1. In summary, DRRZ makes $A_j[k]$ a random sequence, which randomizes the current switch transitions. Thus switching transients are not correlated with the input $M_i[k]$ and will not cause distortion in V_o.

Figure 6 shows the block diagram of proposed 8-bit current-steering DAC. It consist of 8-bit thermometer encoder, Pseudo Random Number Generator (PRNG) and 35 current cells. The DAC is divided into two parts first part consist of 5-bit equally weighted Most Significant Bit (MSB) DAC (M-DAC) comprising of 31 identical current cells each outputs current of 8*I* and second part consist of 3-bit binary weighted Least Significant Bit (LSB) DAC (L-DAC) comprising of four different current cells which outputs current of value 1*I*, 1*I*, 2*I*, and 4*I*, respectively. There are two 1*I* cells in L-DAC so that a differential output of zero can be realized. The nodes i_{o1} and i_{02} of all current cells are tied together to form two differential DAC output terminal. These two output terminal are connected to two R_L to generate output voltage V_{o1} and V_{o2}. When CK is high, encoder controls both M-DAC and L-DAC. The DAC output is expressed as $V_o[k] = (M_i[k]-127)\times 2IRL$, where I = 80 µA and R_L = 25 Ω yields V_o with differential signal range of $1V_{pp}$.

As shown in Figure 6, each current cell consists of MUXES and level sensitive latches. When CK goes low, the latch selects the $A_j[k]$ control from PRNG. The encoder is thermometer encoder and PRNG is a 16-bit linear shift register. PRNGs 16-outputs and their complements form the 32 $A_j[k]$ zero-phase controls. This arrangement ensures that $\sum_{j=1}^{32} A_j[k] = 0$. During the zero phase the entire L-DAC is treated as a single MSB current cell controlled by a single $A_{32}[k]$ signal.
Figure 7 shows the schematic of a current cell. MOSFET P1 and P2 form the cascade current source. MOSFETs P3 and P4 function as current switches. The current source is operated at 2.5 V supply. MOSFET N1-N8 and two inverters form a level-sensitive MUX latch. When CK is high, the $P_j[k]$ signal from encoder is loaded into the latch. When CK is low, $A_j[k]$ signal from PRNG is loaded into the latch. For example when CK is high, and if $P_j[k] = 0$ then current switch N4 will be ON and if $P_j[k] = 1$ then current switch P3 will be ON. The whole MUX- latch operates under 1.2 V supply.

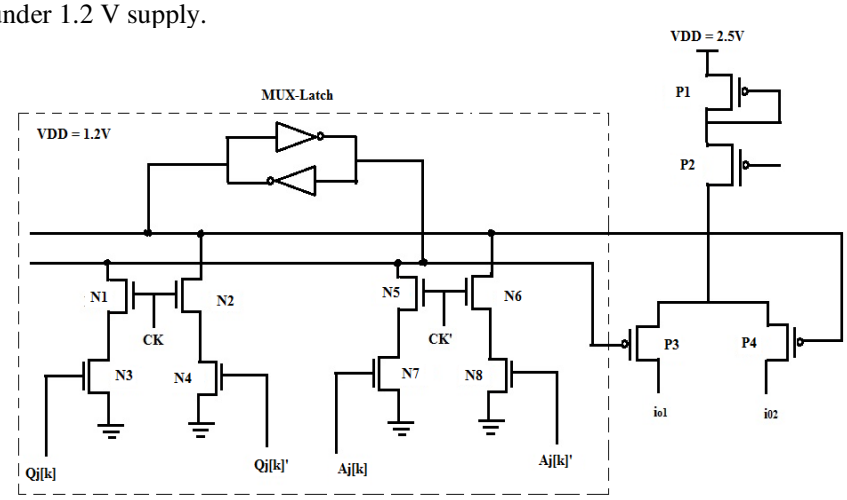

Figure 7. Current cell schematic.

3. RESULTS AND COMPARISON

The DAC is prepared in standard 90-nm CMOS technology. The prepared layout for the same is shown in figure 8. The experimental result are found out to be better as compared to work

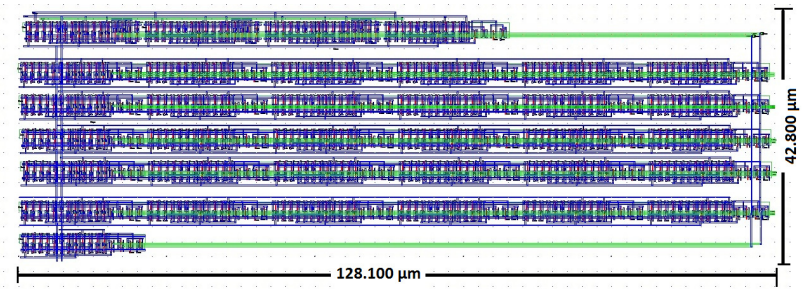

Figure 8. Layout of binary type current steering DAC.

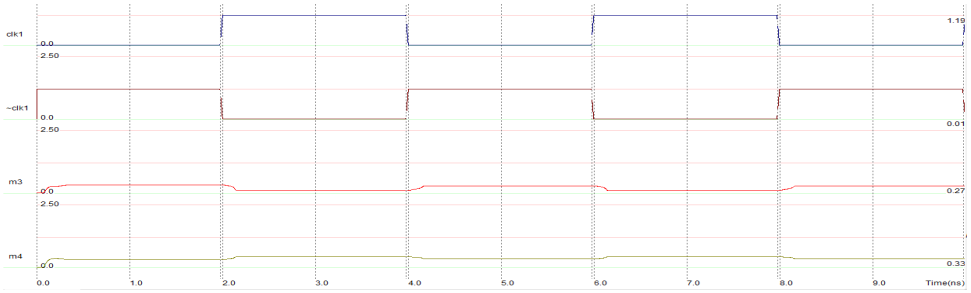

Figure 9. Output waveform of current steering DAC for input 00001011.

published in paper [11]. The output waveform for input of 00001011 is shown in figure 9. There is reduction in power consumption and area occupied, power consumption is 57 mW and DAC core area is 5598 $(\mu m)^2$. The complete DAC performance is shown in Table 1.

Table 1. DAC Performance Summary.

Technology	CMOS 90 nm
Resolution	8 bit
Sampling Rate f_s	1.6 GS/s
Load Current	19 mA
Output Swing	1 *Vpp*
Supply Voltage (Analog/Digital)	2.5 V / 1.2 V
Power Consumption	57 mW
Core Area	5483 $(\mu m)^2$

4. CONCLUSIONS

A CMOS 8-bit binary type current steering DAC is presented to demonstrate the proposed DRRZ technique. This technique requires less power consumption and small overhead in digital circuits.

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