DESIGN OF A BATTERY CHARGER INTERFACE PRE-CHARGE FOR MOBILE PHONE

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ABSTRACT

This paper describes the analysis and design of a Battery Charger Interface Pre-charge (BCIP) for mobile phone. Battery charger interface pre-charge is very important function in the battery management integrated circuit, which allows the control of the charge of the battery with the maximum battery autonomy without reducing its life. The Battery Charger Interface Pre-charge has been designed and implemented in a 0.35µm CMOS technology and the active area of this circuit is about 1.54mm2.

KEYWORDS
Battery charger interface, Pre-charge, Band-gap, Comparator, Shunt-regulator.

1. INTRODUCTION

When designing a circuit for portable applications, an important issue is how to manage the power consumption. Because of the high cost of providing power to portable equipment, the minimization of power dissipation in per line components is a key design objective. low cost integrated battery charging interface is needed to control the charge of the main battery with safety. This interface is more and more integrated with the power management to optimize the battery-autonomy and battery-life [1-2-3-4].

In this paper, we present the new low-cost battery charger pre-charge for the mobile phone. The charging device can be either a charger with a low–output impedance regulated or non-regulated voltage source of 20V absolute maximum or a device plugged in the USB wall outlet. The device plugged in the USB wall outlet can be either a USB driver with a low-output impedance dc voltage source from 4.4V to 5.25V or a carkit with a low-output impedance dc voltage source from 4.75V to 5.25V. Two external PMOS power transistors, driven by ICTLAC2 and ICTLUSB2 of the BCI device, control the choice between the charger input and the USB input. Their role is also to prevent reverse leakage current from the main battery in case of one of the two charging devices is connected to the mobile phone without delivering any voltage at its output. Two external PMOS power transistors driven by ICTLAC1 and ICTLUSB1 of the BCI device, control the current flowing from the charging device to the main battery.

2. DESIGN IMPLEMENTATION OF BATTERY CHARGER INTERFACE

Figure 1 shows the block diagram of the proposed pre-charge circuit, the pre-charge is systematically enabled when a charging device and a battery within the proper ranges are connected. The pre-charge is independent of the battery type and conditioned by the charging

device (i.e. AC charger, USB host, USB charger or carkit). The analog core can perform three different pre-charging schemes.

First a small constant current pre-charging scheme (typically 5mA) is applied automatically to the battery when the battery voltage is lower than 0.5 V. This battery state is attained when the battery is fully discharged, shorted or opened (security activated).

During this mode, the pre-charge architecture sends a constant current to the battery through VCC pin of the battery charge interface (BCI) device.

Then a slow constant current pre-charging scheme is applied automatically to the battery when the battery voltage is higher than 0.5 V. For the USB host devices, this pre-charging scheme is applied when the battery voltage is between 0.5V and 3.6V. For the carkits, the USB chargers and the AC chargers, this pre-charging scheme is applied when the battery voltage is between 0.5V and 2.0V. The value of the slow constant current is 100mA.

During this mode, the pre-charge architecture re-uses the external power components used by the main charge architecture (i.e. dual PMOS and sense resistor). The two external PMOS power transistors driven by ICTLAC2 and ICTLUSB2 of the BCI device control the choice between the AC charger input and the USB input and the two external PMOS power transistors driven by ICTLAC1 and ICTLUSB1 of the BCI device control the current flowing from the charging device to the main battery.

Finally, a fast current dissipation limited pre-charging scheme could be applied to the battery when the battery is between 2.0V and 3.6V and a carkit, a USB charger or an AC charger is connected. The fast current applied is maximum 500mA limited by the external PMOS dissipation. The maximum PMOS dissipation is fixed by 2 external resistors, Rlimitac for th AC pre-charge and Rlimitusb for the USB pre-charge.

During this mode, the pre-charge architecture is the same as the one used for the slow constant current pre-charging scheme but the external Rlimitac or Rlimitusb resistors are connected to limit the external PMOS dissipation.

The BCI can use two modes, the “automatic mode” and the “software control mode”. A boot pin BCIAUTO is implemented to choose between the “automatic mode” and the “software control mode”. For the pre-charge architecture, the difference between the two modes is transparent. In any mode, the pre-charge is automatically stopped when the battery is higher than 3.6V. In any mode the pre-charge is automatically stopped when the power management system is in ACTIVE mode and the software is started (i.e. VBAT>3.2V, SYSACTIV signal is forced to 1). In any mode the pre-charge is automatically re-started when the power management system is in BACKUP mode (i.e. VBAT< 2.8V, SYSACTIV signal is forced to 0).
Then, in the “automatic mode”, the AC or USB charge is automatically started when the power management system is in ACTIVE mode (i.e. VBAT>3.2V, SYSACTIV signal is forced to 1).
The control and the configuration of the analog core are done automatically by the pre-charge Finite State Machine (FSM).

The status block contains six comparators that give the status of the charging devices and the battery. The charger presence comparator detects if a charger is plugged. The associated signal rise when the charger voltage is higher than the battery voltage plus 400mV and fall when the charger voltage is lower than the battery voltage minus 400mV. The battery presence comparator detects if a battery is open. The associated signal rise when the thermistor of the battery pack is connected to the dedicated ADIN pin. The VBUS presence comparator detects if a USB device is plugged. The associated signal rise when VBUS voltage is higher than 0.5V. The end of pre-

charge comparator detects if the battery voltage is higher than 3.6V. The fast pre-charge comparator detects if the battery voltage is higher than 2.0V. The slow pre-charge comparator detects if the battery is higher than 0.5V.

The charger will support a “constant voltage” mode. In this mode, there is no battery pack and a regulated AC charger, a carkit or a USB charger is plugged. The charging device outputs a constant voltage at VBAT node. To start the constant voltage mode, the pre-charge detects first if a battery pack is attached using the battery presence comparator.

The constant voltage mode hardware implementation uses the main charge constant voltage loop. In this mode a 200Ohm load resistor is turned ON to keep the regulated VBAT voltage output stable. The resistor can be disabled by software. In this mode, an external capacitor has to be connected to the VBAT node.

When the conditions to start the constant voltage mode are detected, we have three cases:

Case 1: If the battery node VBAT was lower than 3.2V (no battery pack before charging device plug or battery removal during pre-charge), the slow constant current pre-charging scheme and the fast current dissipation limited pre-charging scheme are disable and the small constant current pre-charging scheme is started. The 5mA will raise the VBAT voltage up to 3.2V (capacitor charge) to let the power management state machine start. The power management state machine will start using the 5mA given by the small current pre-charging scheme. The power management state machine will start using a specific start up sequence (avoid starting all the LDOs and DC DCs before the BCI constant voltage mode is started). When it is started, the power management state machine will send the SYSACTIV signal to the BCI and the BCI AC or USB main charge state machine will start the constant voltage mode using the constant voltage loop.

Case 2: If the battery node VBAT is already higher than 3.2V (battery removal during main charge) and we are in “automatic charge mode”, the hardware of the constant voltage mode is already started because the constant voltage loop is already started.

Case 3: If the battery node VBAT is already higher than 3.2V (battery removal during main charge), we are in “software control mode” and we only have the constant current charge enable. We stop the constant current charge and the system will be shutdown and BCI device will return to pre-charge mode (Case 1).

Case 4: If the battery node VBAT is already higher than 3.2V (battery removal during main charge), we are in “software control mode” and we only have the constant voltage charge enable. The hardware of the constant voltage mode is already started because the constant voltage loop is already started.

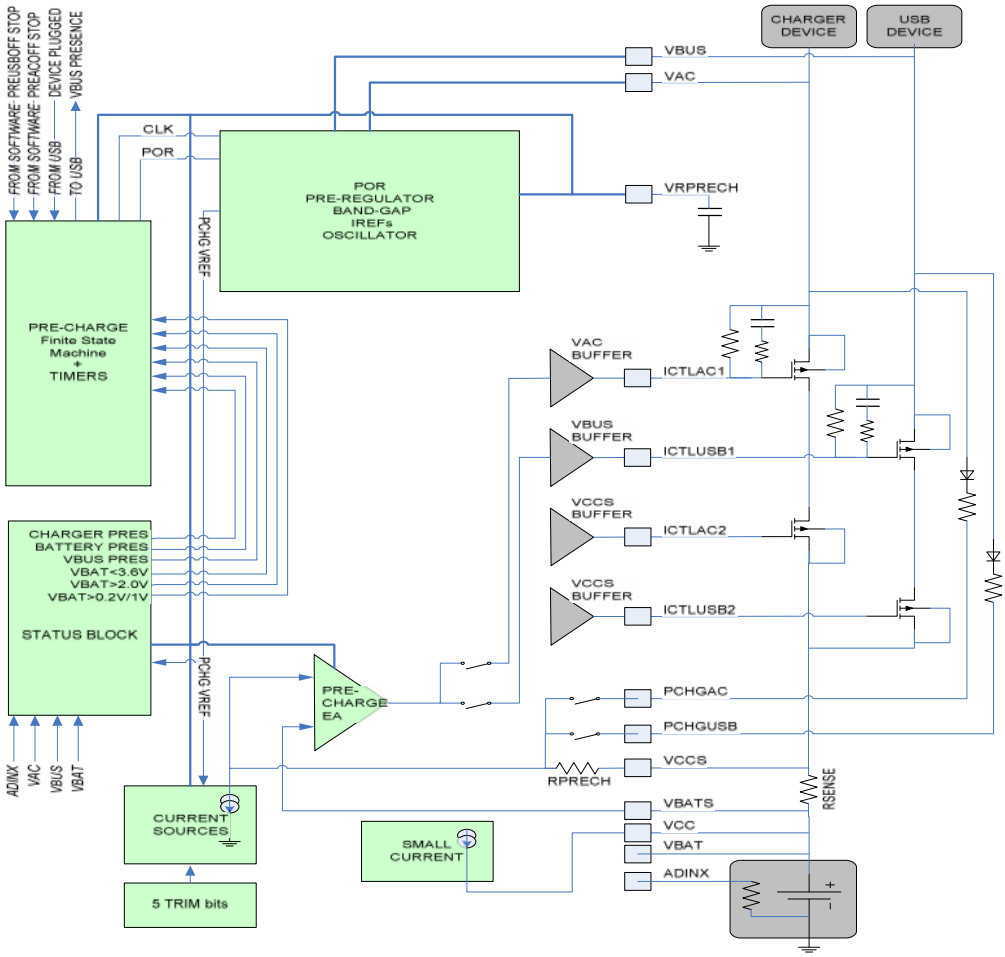


Figure 1: Block diagram of the proposed pre-charge

3. PROPOSED ARCHITECTURE FOR PRE-CHARE

Figure 2 shows the circuit implementation of the proposed pre-charge. The pre-charge has a dedicated power management system. This power management system contains a POR, a pre-regulator, a band gap, an Iref block and an oscillator. The pre-regulator generates a 2.8V output voltage on the VRPRECH pin of the BCI device. This regulated voltage comes from VAC or VBUS pins of the BCI device. The pre-regulator output supplies the current reference, the pre-charge error amplifier, the status block and the pre-charge FSM. The POR sends the associated POR signal to the pre-charge FSM that is used as a reset. POR signal rise when the VRPRECH voltage is higher than 2.0V. The band gap is used to generate the current reference of the slow and fast current dissipation limited pre-charging schemes architectures. The Iref block is used to bias the error amplifier and the status block. The oscillator sends the associated CLK clock signal to the pre-charge FSM.

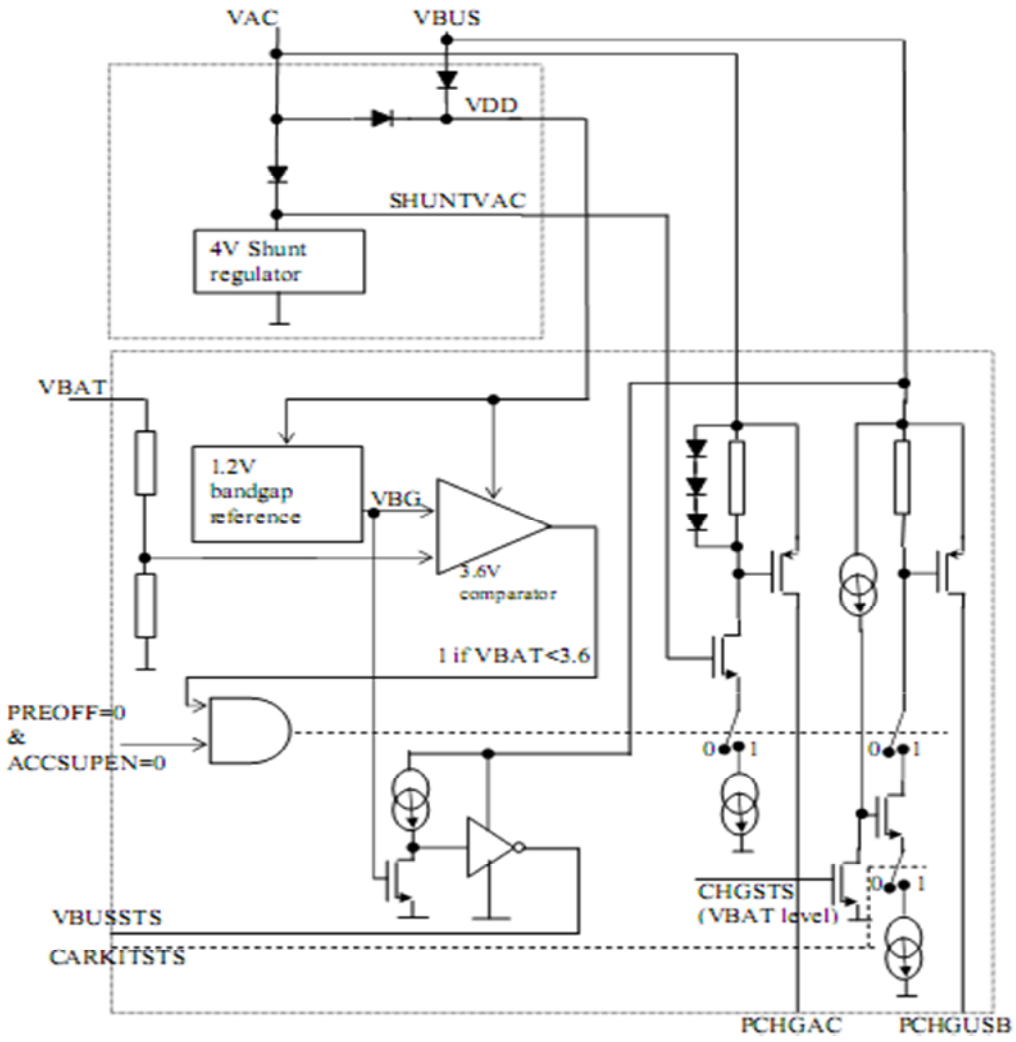


Figure 2: The schematic implementation of proposed pre-charge

In this architecture, the SHUNTVAC voltage is about 4V. It is supplied directly by the VAC voltage. The VDD voltage is the maximum voltage between SHUNTVAC and (VBUS-Vdiode). This supply is used to bias the pre-charge VBG band gap voltage (1.2V typical) and the 3.6V battery voltage comparator. This comparator is used to end the pre-charge from VAC and from VBUS. The VDD current consumption (flowing from VAC or VBUS) is about 50uA. The VBUSSTS signal is high, if the VBG is setup (ie VAC or VBUS is plugged), and VBUS is present. The digital signal is at VBUS level.

In this architecture, there is no 4.4V comparator on VBUS. The advantage for this is a low additionnal current consumption from VBUS: 10uA. If VAC is plugged, CHGSTS is 1 (equal to VBAT), and VSHUNTVAC is about 4V from VAC. Then if VBAT is lower than 3.6V and PREOFF=0 and ACCSUPEN=0, a pre-charge current is sourced from PCHGAC. At the same time, no pre-charge current is sourced from PCHGUSB. This makes the pre-charge from VAC prioritary on the pre-charge from VBUS, when both VAC and VBUS are plugged.

If VAC is not plugged and VBUS is plugged, and VBAT is lower than 3.6V and PREOFF=0 and ACCSUPEN=0, then as soon as the car-kit detector sets CARKITSTS=1 (at level VBUS), a pre-charge current is sourced from PCHGUSB.

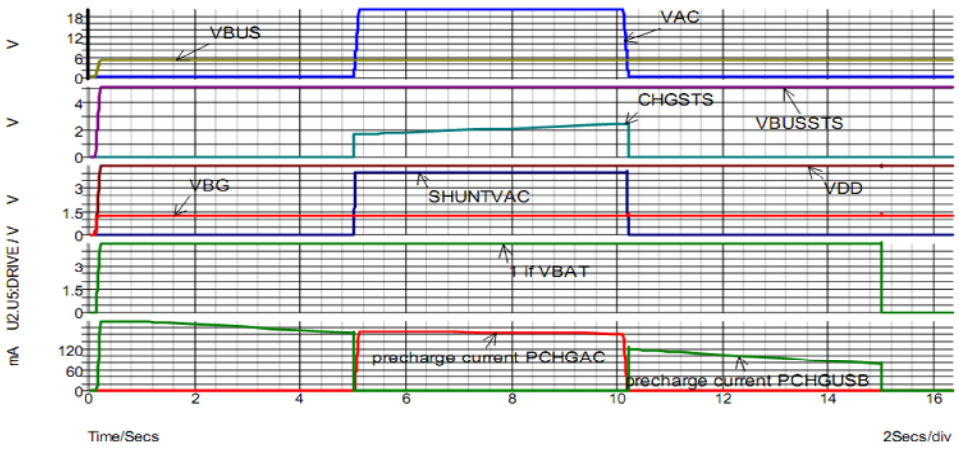


Figure 3: simulation result of pre-charge

The resulting relations of the fast current dissipation limited pre-charging scheme are detailed below. The two relations below gives the pre-charge current (Ichg) function of the pre-charge parameters (Resistances, Reference Current, Devises voltage values).

For the AC pre-charge:

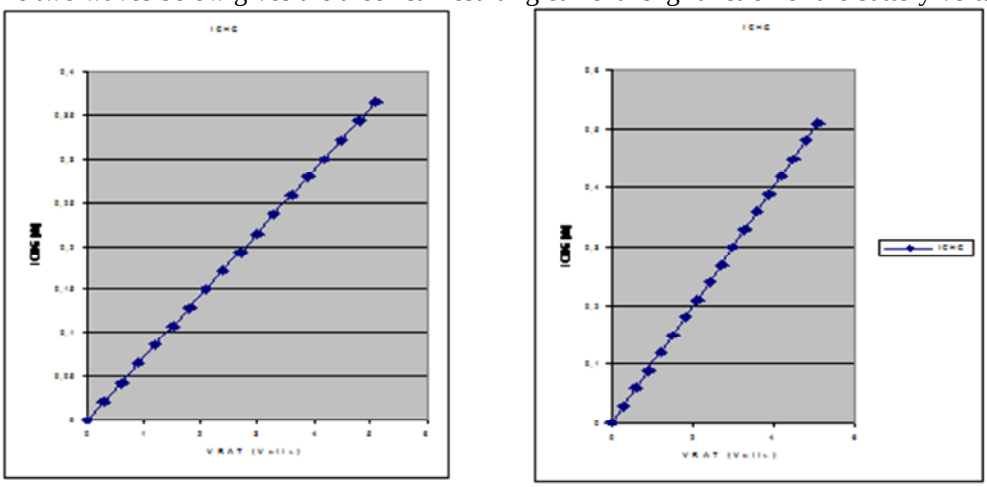
$$Ichg = Iref \times \frac{Rprech}{Rs} - (VAC - VBATS) \times \frac{Rprech}{Rlim\ itac \times Rs} \qquad (1)$$

For the USB pre-charge:

$$Ichg = Iref \times \frac{Rprech}{Rs} - (VBUS - VBATS) \times \frac{Rprech}{Rlim\ itusb \times Rs} \qquad (2)$$

With RS=RSENSE , and Iref the current source reference

The two waves below gives the theorical resulting current Ichg function of the battery voltage.



AC pre-charge with a 7V regulated charger, *Iref*=10uA; *Rprech*=10k; *Rs*=0.2; *Rlimitac*=700k; *VAC*=7V

USB pre-charge with a 5V VBUS *Iref*=10uA; *Rprech*=10k; *Rs*=0.2; *Rlimitusb*=500k: *VAC*=7V

Figure 4: Theorical resulting current Ichg function of the battery voltage

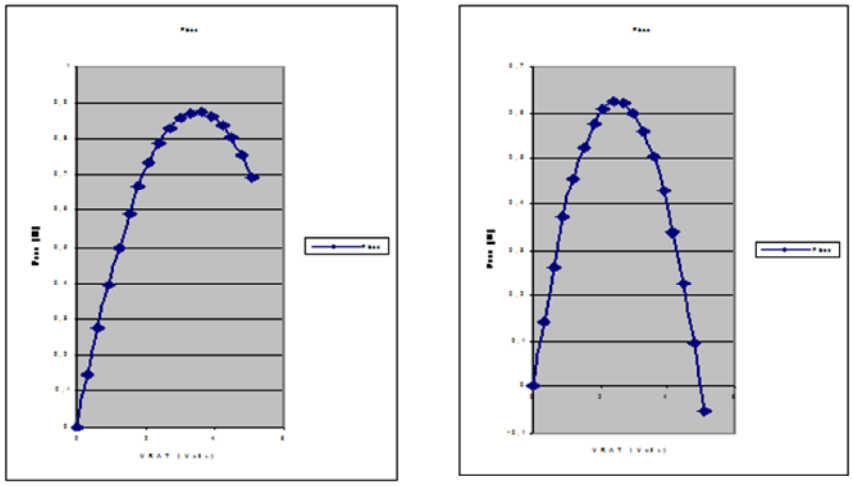
The two relations below gives the power PMOS dissipation (Ploss) function of the pre-charge parameters (Resistances, Reference Current, Devises voltage values).
For the AC pre-charge:

$$Ploss = Vp \cdot Ichg = Vp \cdot Iref \cdot \frac{Rprech}{Rs} - Vp^2 \cdot \frac{Rprech}{Rlimit\,ac \cdot Rs} \quad (3)$$

For the USB pre-charge:

$$Ploss = Vp \cdot Ichg = Vp \cdot Iref \cdot \frac{Rprech}{Rs} - Vp^2 \cdot \frac{Rprech}{Rlimit\,usb \cdot Rs} \quad (4)$$

Where Vp is the power PMOS Drain to Source voltage; Vp=VAC-VBAT or VBUS-VBAT.
The two waves below gives the theorical resulting power PMOS dissipation function of the battery voltage.



AC pre-charge with a 7V regulated charger *Iref*=10uA; *Rprech*=10k; *Rs*=0.2; *Rlimitac*=700k; *VAC*=7V

USB pre-charge with a 5V VBUS *Iref*=10uA; *Rprech*=10k; *Rs*=0.2; *Rlimitusb*=500k; *VAC*=7V):

Figure 5: Theorical resulting power PMOS dissipation function of the battery voltage

4. SIMULATION AND MEASUREMENT RESULTS

Figure. 4 show the layout of the proposed battery charger Interface pre-charge. The active area of this circuit is about 1.54 mm^2 in a 0.35 µm CMOS technology.

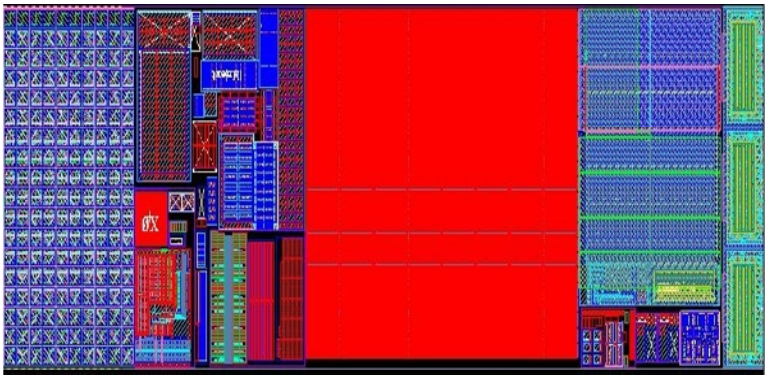


Figure 6: Layout of the proposed BCIP

4.1 Pre-charge VAC

Figure 7 and figure 8. shows the measure VRPRECH for pre-charge VAC and USB .

Measure VRPRECH

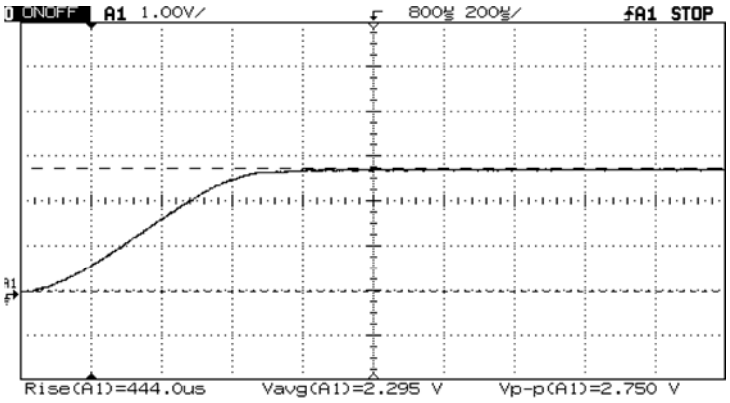


Figure 7: measure VRPRECH for pre-charge VAC

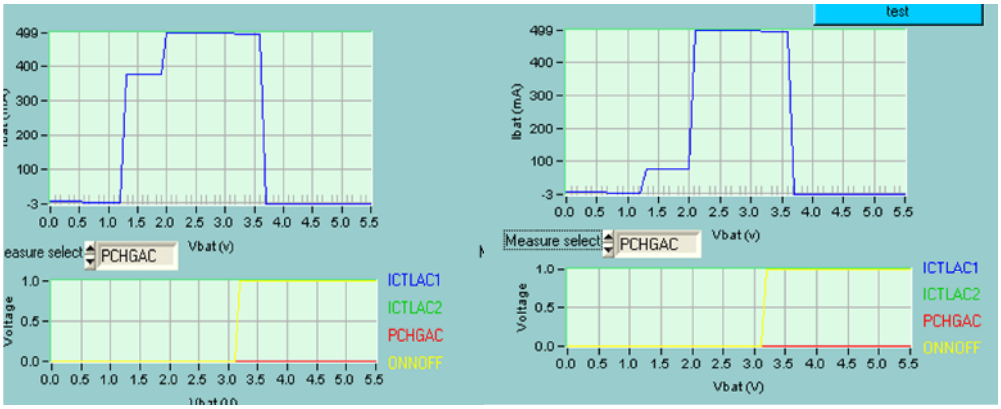


Figure 8: measure Ibat, PCHAC and ONNOFF function of the battery voltage for pre-charge VAC

4.2 Pre-charge USB *Measure VRPRECH*

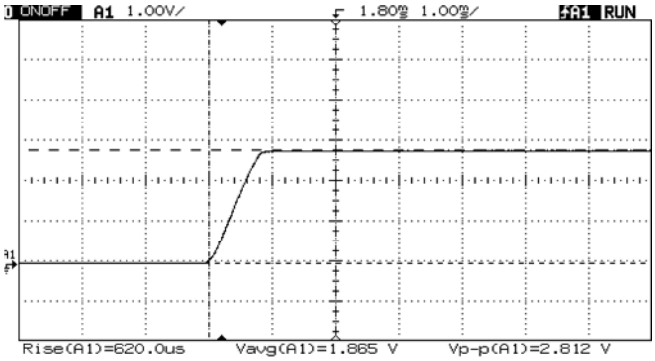


Figure 9: measure VRPRECH for pre-charge USB

4.2.1 Fast per-charger

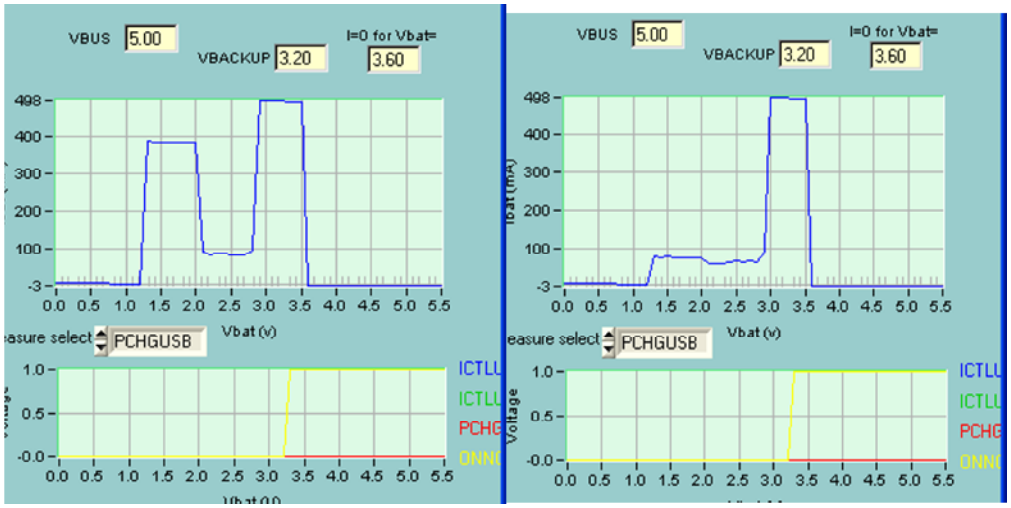


Figure 10: measure Ibat, PCHAC and ONNOFF function of the battery voltage for pre-charge USB

4.2.2 Slow pre-charge

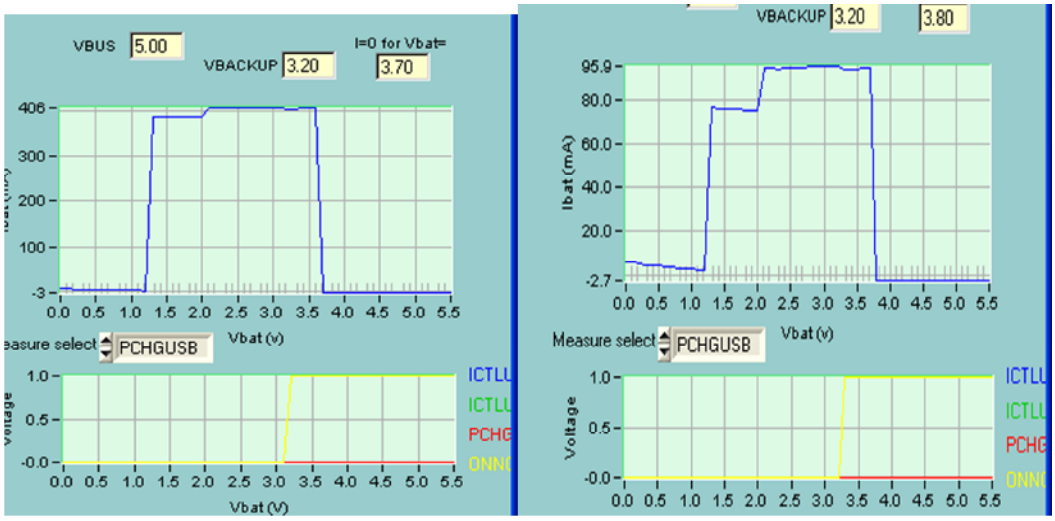


Figure 11: measure Ibat, PCHAC and ONNOFF function of the battery voltage for pre-charge USB

5. CONCLUSIONS

The battery charger interface pre-charge is implemented in a triple metal 0.35µm standard CMOS process capable of supporting battery voltages up to 5.5V. A novel architecture low cost is demonstrated, resulting in a very efficient charging flow with a very accurate end-of-charge mechanism Measurement results show the accuracy. The total area of the BCIP circuits is roughly1.54mm^2.

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