

# SoCs BASED OPENRISC AND MICROBLAZE SOFT PROCESSORS

## COMPARISON STUDY CASES: AUDIO IMPLEMENTATION AND NETWORK IMPLEMENTATION BASED SoCs

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### **ABSTRACT**

*The IP reuse approach and FPGA-platform-based SoC (System on Chip) with an embedded soft processor is an alternative to design SoCs that allows fast creation and verification. In this paper we address a comparison study between two SoCs architectures based OpenRISC (OpenCores) and MicroBlaze (proprietary) soft processors. The comparison is done for two applications, namely the audio and network applications based SoCs. The SoCs have been prototyped using the Virtex5 XC5VLX50 FPGA. Regarding the SoCs for audio application, the results show that slices are more used in the OpenRISC based SoC while BRAM memories are more used in the SoC based MicroBlaze. Concerning the SoCs for Network application used slices register are slightly different in the two SoCs, BRAM memories and slice LUTs are more used in the OpenRISC based SoC. We notice that power consumption is better for the SoCs based MicroBlaze for the both applications.*

### **KEYWORDS**

*Audio, AC97 controller, Embedded system, FPGA, MicroBlaze, Power consumption, System on Chip (SoC), OpenCores, OpenRISC*

## **1. INTRODUCTION**

SoC concept is based on integrating all components involved in the design in a single chip. Several and critical design constraints are involved when designing SoCs. Namely power consumption, area usage, device size, chip interconnection, design cost (this constraint is critical, mainly for academic research) and time to market. All aspects related to SoCs concept are given in [1]. To overcome the increasing complexity to design SoCs, embedded system developers seek for solutions allowing flexibility and efficiency. The Soft processor based platform for designing SoCs is an attractive way for implementing embedded applications, while reducing power consumption and design cost compared to ASIC. Soft processor is a hardware description language (HDL) model of a specific processor (CPU) that can be customized for a given application and synthesized for an ASIC or FPGA target [2]. There are several soft processor provided by commercial vendors, namely Nios processor, Xilinx MicroBlaze processor and PicoBlaze microcontroller, the IBM processor and Xtensa by

respectively Altera, Xilinx, IBM, Tensilica. Other soft processors are Opensources provided by Opensource community, namely the OpenRISC processor by OpenCores and LEON by Gaisler Research. Both of Opensource and proprietary soft processors are used in academic and industrial research to design embedded systems. A comparison study has been done by Jason G et al. [2] and [3], where several soft processors are presented and compared. In this work we focus on the OpenRISC and MicroBlaze processors since the SoCs compared herein are based on these two processors for the both applications: namely the audio and network applications used as cases study. In SoC for audio application, the processor read and plays back audio using the AC97 controller, through the line out audio port. The SoC based OpenRISC is a part of the SoC platform based on Opencores and Opensources design concepts for Voice over Internet Protocol application [4] [5]. A presentation of the OpenRISC and MicroBlaze soft processors is given in previous work [6] that exposes a comparison study between two SoCs architectures based OpenRISC and MicroBlaze for network application [7] and [8].

In Section II, we give features comparison of the two soft processors. Section III, deals with the Hardware architectures of the two SoCs for audio application. The synthesis and implementation results for both OpenRISC and MicroBlaze based SoCs for audio applications are given in this section. In Section IV, The synthesis and implementation results for the two SoCs for network applications are exposed. Finally, we give a conclusion in section V.

## 2. FEATURES COMPARISON OF THE TWO SOFT PROCESSORS

Table 1 shows a comparison of the two soft processors namely the OpenRISC and MicroBlaze. The results summarized in table I show that, the MicroBlaze processor has a highest operating frequency than the OpenRISC processor in FPGA target, while the OpenRISC has higher operating frequency for ASIC target. MicroBlaze is Xilinx proprietary, so it is targeted for Xilinx FPGA only, while OpenRISC is technology independent, it can be implemented in different FPGA (it is implemented in Xilinx and Altera FPGA) or ASIC target. The two processors have the FPU unit included in their architectures. Regarding the area, the OpenRISC uses more LUTs than the MicroBlaze.

Table 1. Features Comparison

Features	OpenRISC 1200	MicroBlaze(Xilinx)
License	Opensource (GPL)	Proprietary (Xilinx)
Pipeline depth	5	3/5
Architecture	32-bit RISC	32-bit RISC
Speed MHz	250(ASIC)/60 (5VLX50 FPGA)	235MHz (5VLX50 FPGA)
Area LUTs	4125 LUTs	1027 LUTs
Implementation/technology	FPGA/ASIC 0.18 $\mu$ m	Xilinx FPGA only
FPU	IEEE 754	IEEE 754
Performance DMIPs	250 DMIPs	280 DMIPs

### 3. AUDIO SoCs HARDWARE ARCHITECTURE PRESENTATION

#### 3.1. OpenRISC based SoC Hardware Architecture for audio application

Figure 1 shows the block diagram of the SoC architecture based OpenRISC soft processor. The embedded SoC includes OR1200 core and a minimum set of elements needed to provide functionality of audio application. These elements are the debug unit for debugging purpose, a memory controller that controls an external memory, a Universal Asynchronous Receiver Transmitter (UART), the MAC/Ethernet that transmits voice packets over the Internet. All the cores are connected through the wishbone bus interface. The AC97 controller core is also selected for audio processing application. For the integration of all the cores we have created a SoC Verilog description.

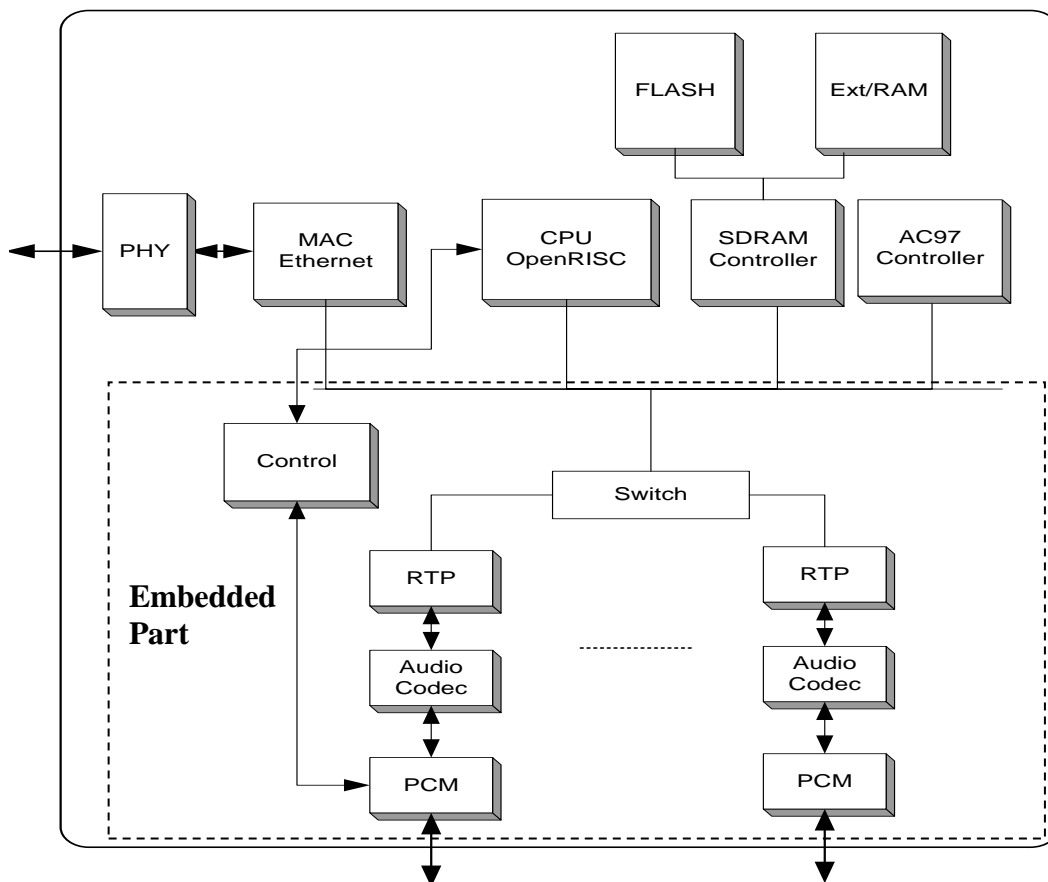


Figure 1. SoC based OpenRISC hardware architecture for audio application

#### 3.2. System based OpenRISC Prototyping

The architecture has been prototyped using the Xilinx development platform ML501-Virtex5, The operating frequency is 66MHz. The development tool used for the design and implementation is ISE 13.1 tool by Xilinx [9]. Table 2 summarizes the synthesis results. The SoC uses 63% of BRAM memories, 55 % of slices. It is noticeable that the BRAM memories are the most used resources. The power estimation is done using the XPower Analyzer by Xilinx [10] which support detailed power estimation based on characterized resource capacitance, design-specific resource utilization and data switching activity. Table 3 summarizes the power consumption of the design; the total power consumption is 5.160W.

Table 2. Synthesis results (SoC based OpenRISC).Target device XC5VLX50- 1FF676

Slice Logic resources	Used Slice Logic	Available Slice Logic	% Occupied resources
Used Slice	15979	28800	55
Number of bonded IOBs	174	440	40
Number of BRAMs	30	48	63

Table 3. Power consumption (SoC based OpenRISC)

Total estimated power consumption	Power (W)
Logic	0.003
IO (W)	3.203
BRAM (W)	0.022
Quiescent	4.686
Dynamic (W)	0.474
Total(W)	5.160

### 3.3. MicroBlaze Based SoC Hardware Architecture for audio application

Figure 2 shows the block diagram of the SoC architecture based MicroBlaze soft processor for audio application [11]. The SoC is designed using Xilinx EDK platform. The Hardware architecture includes mainly, the MicroBlaze core, an AC97 module, UART and the Ethernet EMC.

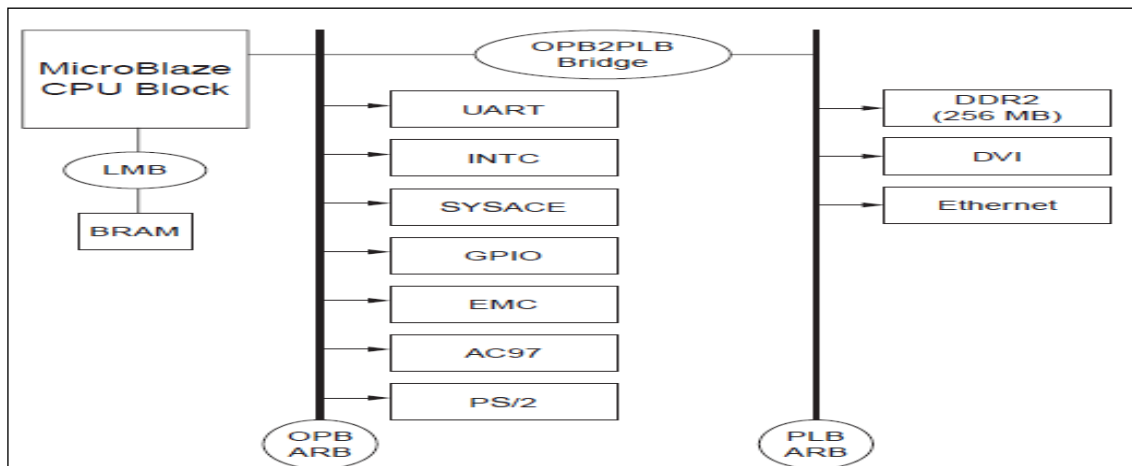


Figure 2. SoC based MicroBlaze hardware architecture for audio application

### 3.4. System based MicroBlaze Prototyping

The same tools and target are used to prototype the architecture of the SoC based MicroBlaze. As shown in table 4 the SoC uses 75% of BRAM memories, 34% of slices. Table 5 summarizes the power consumption of the design; the total power consumption is 4.046W.

Table 4. Synthesis results (SoC based MicroBlaze) target device xc5vlx50-1ff676

Slice Logic resources	Used Slice Logic	Available Slice Logic	% Occupied resources
Slice registers	9897	28800	34
Number of bonded IOBs	261	440	59
Number of BRAMs	36	48	75

Table 5. Power consumption (SoC based MicroBlaze)

Total estimated power consumption	Power (W)
Logic	0.003
IO (W)	2.016
BRAM (W)	0.120
Quiescent	3.498
Dynamic (W)	0.547
Total(W)	4.046

### 3.4. Features comparison of the two SoCs for audio application

The Xilinx (ISE and XPower) tools are used for both SoCs; we have targeted the virtex5 XC5VLX50 FPGA. Results presented in table 6 show that the OpenRISC-based SoC uses 55 % of FPGA resources. The total power consumption is 5.160 W; the dynamic power consumption is about 0.474 W and 4.686 W for quiescent power consumption. It is noticeable that the BRAM memories are the most used resources. The MicroBlaze-based one uses 34 % slices. The total power consumption is 4.046 W; the dynamic power consumption is about 0.547 W and 3.498 W for quiescent power consumption. The results show that slices are more used in the OpenRISC based SoC while BRAM memories are more used in the SoC based MicroBlaze. Power consumption is better for the SoC based MicroBlaze.

Table 6. Features comparison of the two SoCs for audio application

Features	OpenRISC 1200 based SoC	MicroBlaze (Xilinx) based SoC
Slice	55%	34%
Number of bonded IOBs	40%	59%
Number of BRAMs	63%	75%

Power consumption Total(W)	5.160	4.046
Dynamic (W)	0.474	0.547
Quiescent	4.686	3.498
BRAM (W)	0.022	0.120

#### 4. NETWORK SoCs PROTOTYPING

Figures 3 and 4 show respectively the hardware architecture of the network SoC architecture based OpenRISC and MicroBlaze based one [6].

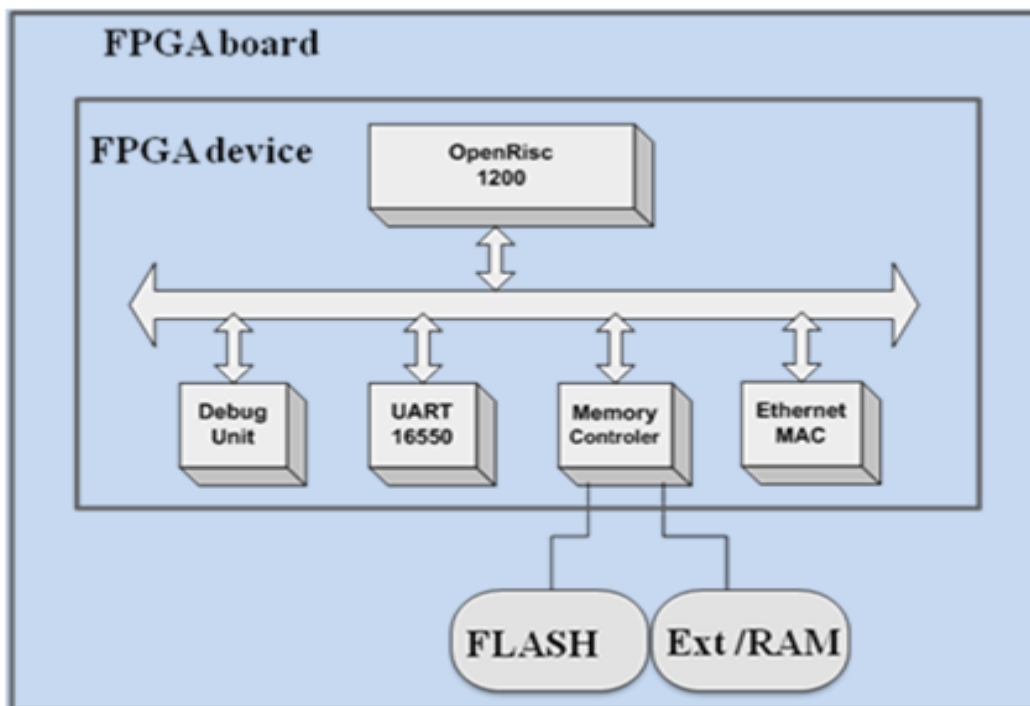


Figure 3. Network SoC based OpenRISC hardware architecture

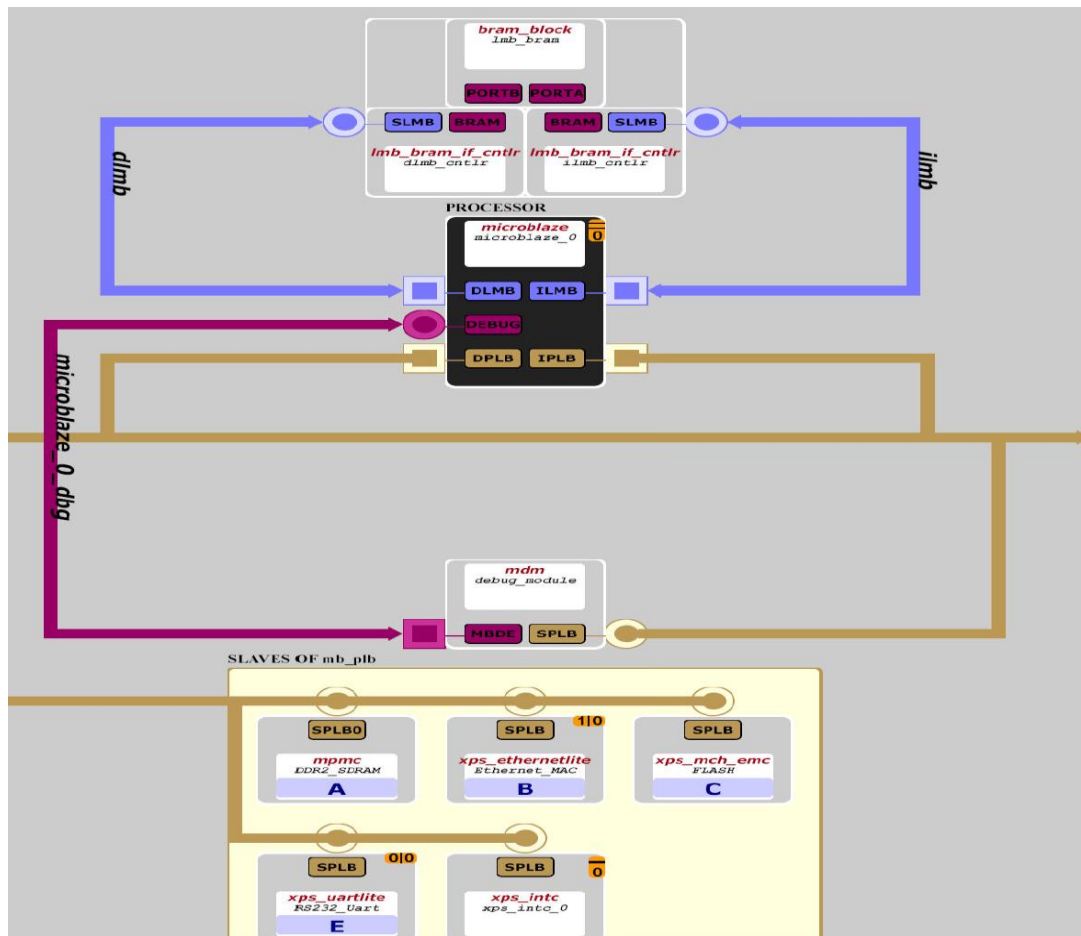


Figure 4. Network SoC base MicroBlaze hardware architecture

#### 4.1. System based OpenRISC Prototyping

The same tools and target are used to prototype the architecture of the SoCs for network application. Table 7 shows the synthesis results. The SoC uses 50% of BRAM memories, 27 % of slice registers and 48% of slice LUTs. It is noticeable that the BRAM memories are the most used resources, the use of other resources remain low. Table 8 summarizes the power consumption of the design; the total power consumption is 4.233 W.

Table 7. Synthesis results (SoC based OpenRISC).Target device XC5VLX50- 1FF676)

Slice Logic resources	Used Slice Logic	Available Slice Logic	% Occupied resources
Slice registers	7864	28800	27%
Slice LUTs	13872	28800	48%
Number of bonded IOBs	192	440	43%
Number of BRAMs	24	48	50%

Table 8. Power consumption (SoC based OpenRISC)

<b>Total estimated power consumption</b>	<b>Power (W)</b>
Logic	0.009
IO (W)	3.346
BRAM (W)	0.053
Quiescent	3.839
Dynamic (W)	0.394
Total(W)	4.233

#### 4.2. System based MicroBlaze Prototyping

As shown in table 9 the SoC uses 16% of BRAM memories, 22 % of slice registers and 21% of slice LUTs. The operating frequency is 171.527 MHz. Table 10 summarizes the power consumption of the design; the total power consumption is 3.677W.

Table 9. Synthesis results (SoC based Microblaze) Target device XC5VLX50-1FF67)

<b>Slice Logic resources</b>	<b>Used Slice Logic</b>	<b>Available Slice Logic</b>	<b>% Occupied resources</b>
Slice registers	6576	28800	22%
Slice LUTs	6155	28800	21%
Number of bonded IOBs	88	440	20%
Number of BRAMs	8	48	16%

Table 10. Power consumption (SoC based Microblaze)

<b>Total estimated power consumption</b>	<b>Power (W)</b>
Logic	0.003
IO (W)	1.872
BRAM (W)	0.064
Quiescent	3.340
Dynamic (W)	0.337
Total(W)	3.677

#### 4.3. Features comparison of the two SoCs for network application

Results presented in table 11 show that the OpenRISC-based SoC for network application uses 27 % slice register, 48% of LUTs, 43 % of IOB and 50% of BRAM memories. The total power consumption is 4.233 W; the dynamic power consumption is about 0.394 W and 3.839 W for quiescent power consumption. It is noticeable that the BRAM memories are the most used resources, the use of other resources remain low. The MicroBlaze-based one uses 22 % slice register, 21% of LUTs, 20 % of IOB and 16% of BRAM memories. The total power consumption is 3.677 W; the dynamic power consumption is about 0.337 W and 3.340 W for quiescent power consumption. We notice that power consumption is better for the SoC based MicroBlaze.

Table 11. Features comparison of the two SoCs for network application



Features	OpenRISC 1200 based SoC	MicroBlaze (Xilinx) based SoC
Slice registers	27%	22%
Slice LUTs	48%	21%
Number of bonded IOBs	43%	20%
Number of BRAMs	50%	16%
Power consumption Total(W)	4.233	3.677
Dynamic (W)	0.394	0.337
Quiescent	3.839	3.340
BRAM (W)	0.053	0.064
Logic	0.009	0.003

## 5. CONCLUSIONS

SoCs based soft processors, namely OpenRISC-based SoC and MicroBlaze-based one are presented in this paper. Two comparison cases study are given. The first case is the audio application the second is the network application based SoCs. In the SoCs for audio application, the slices are more used in the OpenRISC based SoC while BRAM memories are more used in the SoC based MicroBlaze. For the Network application based SoCs, used slice registers are slightly different, BRAM memories and slice LUTs are more used in the OpenRISC based one.

The total power consumption is 5.160W for the SoC based OpenRISC for audio application and 4.046 W for the MicroBlaze based one. Regarding the SoC for Network application, the total power consumption is 4.233 W for the SoC based OpenRISC and 3.677 W for the MicroBlaze based one. We notice that power consumption is better for the SoC based MicroBlaze for the both applications. In FPGA target, the MicoBlaze processor has a highest operating frequency than the OpenRISC processor which is more efficient in ASIC implementation with 250 MHz. MicroBlaze is Xilinx proprietary, targeted for Xilinx FPGA only, while OpenRISC is an Opensource IP-core freely available and technology independent, it can be implemented in different FPGA or ASIC. The Register Transfer Level (RTL) descriptions for all the IPs components included in the proposed SoCs based OpenRISC are free, so it is mainly suitable for academic research.

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