

INVERTING BUCK-BOOST DCDC CONVERTER DESIGN CHALLENGES

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ABSTRACT

This paper presents an inverting buck-boost DCDC converter design. A negative supply voltage is needed in a variety of applications, but only a few DCDC converters are available on the market. OLED, a new display type especially suited for small digital camera or mobile phone displays. Design challenges that came up when negative voltages have to be handled on chip will be discussed, such as continuous/discontinuous mode transition problems, negative voltage feedback and negative over-voltage protection. Both devices operate in a fixed frequency PWM mode or alternatively in PFM mode. The single inductor topology is called inverting buck-boost converter or simply inverter. The proposed converter has been implemented with a TSMC 0.13-um 2P4M CMOS process, and the chip area is 325 x 300 um².

KEYWORDS

Buck-boost converter, DCM / CCM detection, Negative supply voltage.

1. INTRODUCTION

DCDC converters are needed in many battery powered portable products. The battery voltage varies with load and battery lifetime. Alkaline, Ni-MH, Ni-Cd, Lithium and Lithium-Ion batteries are widely used today [1]-[2]. Some of them are rechargeable, some are not. Depending on the application requirements, various DCDC converter concepts are used that regulate the battery voltage to a fixed desired voltage. Linear voltage regulators have been used for a long time, but today charge pumps or inductive switch mode power supplies are preferred because of their higher efficiency [3]-[4]. Also, switch mode power supplies can generate lower or higher voltages, while linear regulators only can regulate to lower voltage values [5]. Inductive converters can easily control output currents from almost zero up to several amps. There are voltage mode and current mode converters, continuous and discontinuous operating modes, constant frequency, constant on time, constant off time and hysteretic operation, PWM and PFM control techniques [6]-[7]. This paper is about design challenges for a voltage mode, constant frequency PWM inverting buck-boost converter intended to generate a negative output voltage from a positive input voltage. The converter operates with a fixed frequency PWM control topology and, if power-save mode is enabled, it uses a pulse-skipping mode at light load currents. It operates with only 500- μ A device quiescent current. Independent enable pins allow power up and power down sequencing for both outputs. The device has an internal current limit overvoltage protection and a thermal shutdown for highest reliability under fault conditions.

2. INVERTING BUCK-BOOST CONVERTER TOPOLOGY

A buck converter decreases an input voltage. At least one switch at the input is required to connect the input voltage to one side of the inductor. Another switch at the same side of the inductor switches to ground in the off state or alternatively, a diode takes over the decreasing inductor current. The other side of the inductor is permanently connected to the output. A capacitor has to be in place at the input and at the output for stability reasons and to limit huge voltage drops upon fast load transients. A boost converter increases an input voltage. At least one switch at the output is required to connect one side of the inductor to ground.

Another switch at the same side of the inductor switches to the output in the off state or alternatively, a diode takes over the decreasing inductor current. The other side of the inductor is permanently connected to the input. A buck-boost converter basically is a combination of a buck and a boost converter. There are normally two switches at the input and two switches at the output. It can either increase or decrease the input voltage. An inverting buck-boost converter has only one switch at the input and one switch or a diode at the output. But, to be honest, since integrated circuits usually cannot handle negative voltages, the switch at the output cannot be used. The diode becomes a necessity. Therefore, sometimes a slightly modified boost converter is used and another inductor and another capacitor are arranged as shown in fig. 1 to generate a negative output voltage.

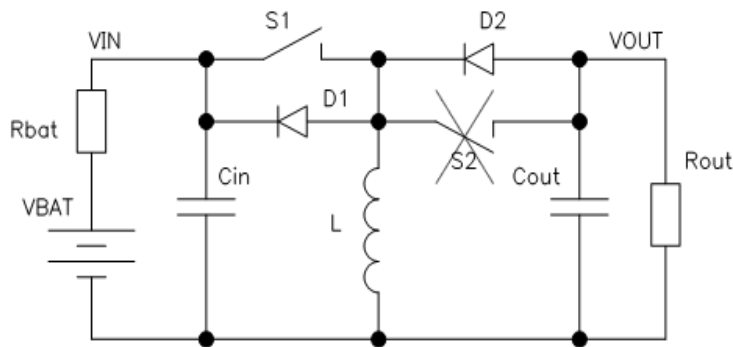


Figure.1. Simple buck-boost converter topology

The inverter discussed in this paper does not require two inductors but uses the simple one inductor concept shown in fig. 1. Diode D1 just indicates that there is a parasitic pn-junction associated with the PMOS switch S1 which is the only component in figure that is on chip. The rest are all external components. D2 is expected to be a schottky diode. Rout represents the load which could be replaced by a current source Iload. S1 has to be controlled such that the desired voltage VOUT remains stable under all VIN and Iload conditions. In continuous current mode CCM operation the inductor current never reaches zero or goes below zero. S1 is turned on and off with a constant frequency. The duty cycle D determines the output voltage according to equation (1) or (2).

$$VOUT = -VIN \times \frac{D}{1 - D} \quad (1)$$

Let D1 be the duty cycle ton/T, for which the switch S1 is on and let D2 be toff/T for which the inductor current continues to flow through diode D2. In CCM D1+D2=1 or D2=1-D1.

$$V_{OUT} = -V_{IN} \times \frac{D1}{D2} \quad (2)$$

In order to maintain V_{OUT} constant, the duty cycle has to be controlled accordingly. The equation could be solved either for $D1$ or for $D2$. Since $D1$ and $D2$ are directly dependent on each other, it does not matter which one of the two are controlled. This means, that if we can set the off time according to equation (3), V_{OUT} stays constant. Of course, this is true for any value of V_{OUT} . Therefore, the off time has to be changed immediately from (3) when V_{OUT} changes e.g. due to load variations. Also, it will never be possible to set the off time accurate enough just by T , V_{IN} and V_{OUT} . According to (3), the off time would follow a V_{IN} change perfectly and V_{OUT} would stay unchanged. But, there will always be some regulation that fine tunes the off time.

$$toff = T \times \frac{V_{IN}}{V_{IN} - V_{OUT}} \quad (3)$$

Figure 2 shows three paths that influence the off time. The “toff control” and “osc” blocks each use the same type of matched capacitor, which is charged via a current to a reference voltage proportional to V_{IN} .

The current used in the oscillator is also proportional to V_{IN} in order to keep T constant. The current in the “toff control” block is made proportional to $V_{IN}-V_{OUT}$ so that toff is approximately correct even under open loop conditions. Two additional regulation loops control the off time. One loop is as fast as possible and has to be designed with the constraint to keep the loop stable. The other loop is compensated externally by a big capacitor and is very slow. It has a very high DC gain and assures high accuracy.

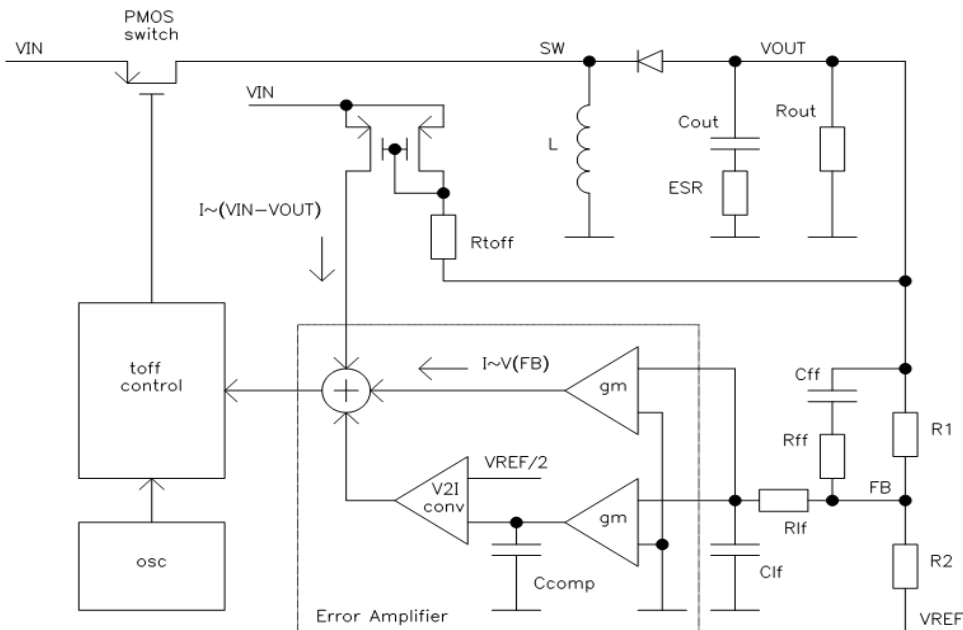


Figure.2. Off time control loop

As can be seen also in figure 2, the error amplifier regulates the FB pin to 0V. This is possible when the voltage divider that monitors VOUT is connected between VOUT and VREF instead of VOUT and GND.

As a result, although sensing a negative voltage, no negative voltage value has to be applied to the chip.

3. DISCONTINUOUS OPERATION ISSUES

Usually, in the application the load changes between no load and very high peaks that can be covered only by the load capacitor. Current limit circuits protect the chip in overstress or short circuit cases. Reducing the load would result in negative current flow but due to the presence of D2, the inductor current becomes zero. Figure 3 shows a CCM example, while figure 4 shows DCM inductor current and switch pin SW behavior.

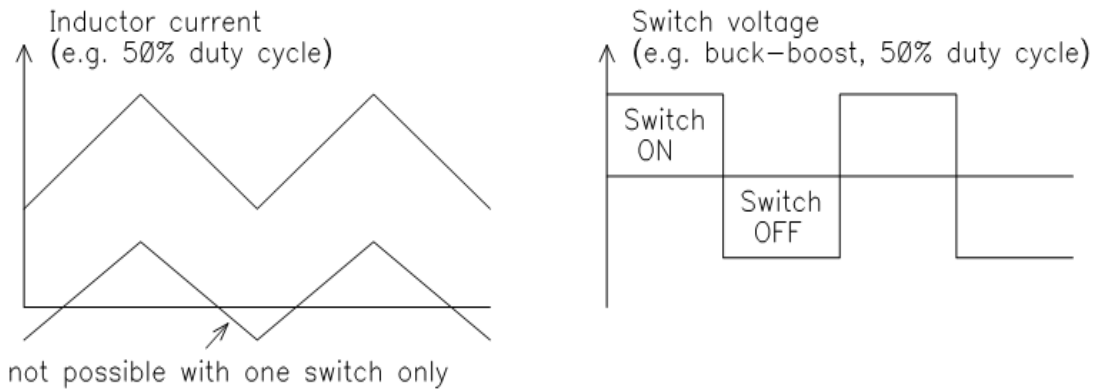


Figure.3. Continuous conduction mode CCM

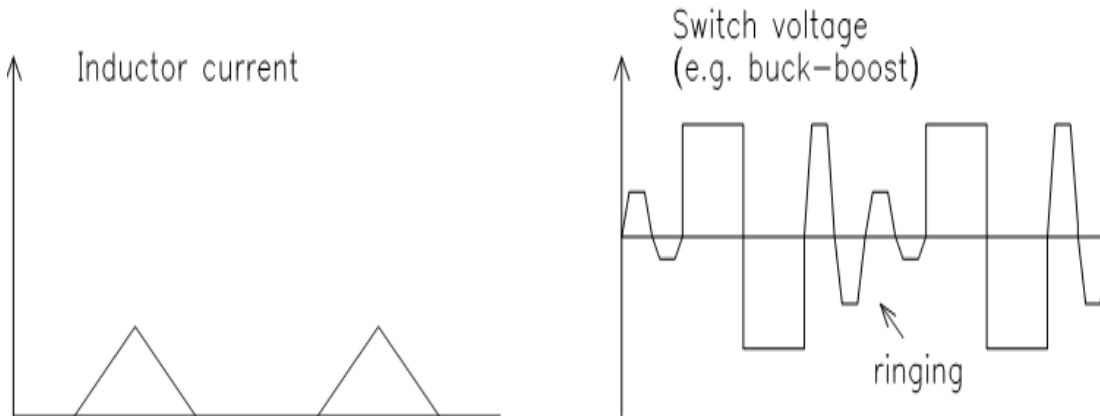


Figure. 4. Discontinuous conduction mode DCM

In contrast to CCM where the off time is independent of the load, the off time in discontinuous mode no longer follows equation (3). With $D1 \times T$ being the time for which the switch is on and

$D2 \times T$ being the time for which the diode conducts, $D1 + D2$ is no longer equal to 1. As mentioned earlier, it is not possible to use a switch instead of a diode for an inverter. A NMOS device cannot be connected to a negative voltage. The pn-junction to the substrate would clamp the voltage to about -0.7V. A PMOS device would have to be controlled by negative voltages below V_{OUT} to turn it on which is not possible, too. Even if NMOS devices could be isolated from substrate, there is no way to turn it off with normal logic levels. Level shifting to $-V_{OUT}$ is not really a solution to control big switches. Thus, the diode cannot be replaced by a switch which automatically forces discontinuous operation at light loads. Now, since discontinuous operation cannot be avoided, let us derive the equation that is valid for the off time in that mode.

As can be seen in figure 4, $(D1 + D2) < 1$. The net volt-seconds area across the inductor is zero.

$$V_{IN} \times D1 \times T + V_{OUT} \times D2 \times T = 0 \quad (4)$$

Solving for V_{OUT} results in

$$V_{OUT} = -V_{IN} \times \frac{D1}{D2} \quad (5)$$

One way to determine $D1$ or $D2$ is to consider the power balance between the input and output. With the average input current I_{IN} and the average output current I_{OUT} and 100% efficiency

$$V_{IN} \times I_{IN} = V_{OUT} \times I_{OUT} \quad (6)$$

Using equation (5)

$$I_{IN} = -I_{OUT} \times \frac{D1}{D2} = \frac{-V_{OUT}}{R_{OUT}} \times \frac{D1}{D2} = \frac{V_{IN}}{R_{OUT}} \times \left(\frac{D1}{D2}\right)^2 \quad (7)$$

The average input current plus the average output current is the same as the average inductor current. Let the peak inductor current be ΔI_L and the period for which this current flows is $(D1 \times T + D2 \times T)$. This period is the base of a triangle that defines the inductor current. The average inductor current is obtained as the area of this triangle divided by the clock cycle period.

$$I_{IN} = \Delta I_L \times \frac{D1 + D2}{2} - I_{OUT} \quad (8)$$

Equating equations (7) and (8) delivers

$$\Delta I_L = \frac{2 \times -V_{OUT}}{R_{OUT} \times D2} \quad (9)$$

Also, we know

$$\Delta I_L = \frac{D1 \times T \times V_{IN}}{L} = \frac{D1 \times V_{IN}}{f \times L} = \frac{D2 \times -V_{OUT}}{f \times L} \quad (10)$$

Substituting for ΔI_L from equation (10) in (9) we get

$$\frac{D2 \times -V_{OUT}}{f \times L} = \frac{2 \times -V_{OUT}}{R_{OUT} \times D2} \quad (11)$$

Equation (11) can be re-written as

$$(D2)^2 = \frac{2 \times f \times L}{R_{OUT}} \quad (12)$$

Solving for D2

$$D2 = \sqrt{\frac{2 \times f \times L}{R_{OUT}}} \quad (13)$$

The off time, our parameter to be regulated is

$$t_{off} = T \times (1 - D1) \quad (14)$$

Substituting for D1 from equation (5) and for D2 from equation (13) we get

$$t_{off} = T - \frac{-V_{OUT}}{V_{IN}} \times \sqrt{\frac{2 \times T \times L}{R_{OUT}}} \quad (15)$$

As can be seen easily when we compare equations (3) and (15), the off time behaves very differently in continuous and discontinuous operation. Equating D2 in continuous mode which can be derived from equation (3) with the expression for D2 in (13) and solving for R_{OUT} gives the CCM/DCM transition point value for R_{OUT}.

In discontinuous mode, the error amplifier has more work to do in regulating load changes. As a result, the fast error amplifier path is not able to regulate out fast load changes whenever CCM OR DCM regulation is left or entered. It takes a while to bring V_{OUT} back to the desired value via the slow, high gain error amplifier path. Huge output voltage drops can occur due to sudden load jumps as can be seen in figure 5 where V_{OUT} has been measured when the output load suddenly changes from 10mA to 120mA. A drop of 2.5V with V_{OUT}=-12V means about 20%. Figure 6 shows the V_{OUT} overshoot from 120mA back to 10mA.

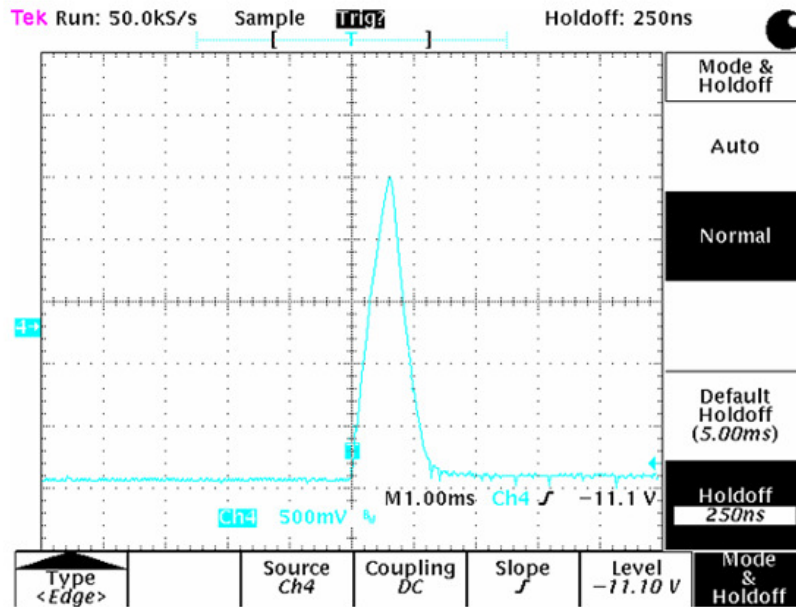


Figure .5. VOUT voltage drop from -12V to -9.5V upon sudden load change from 10mA to 120mA

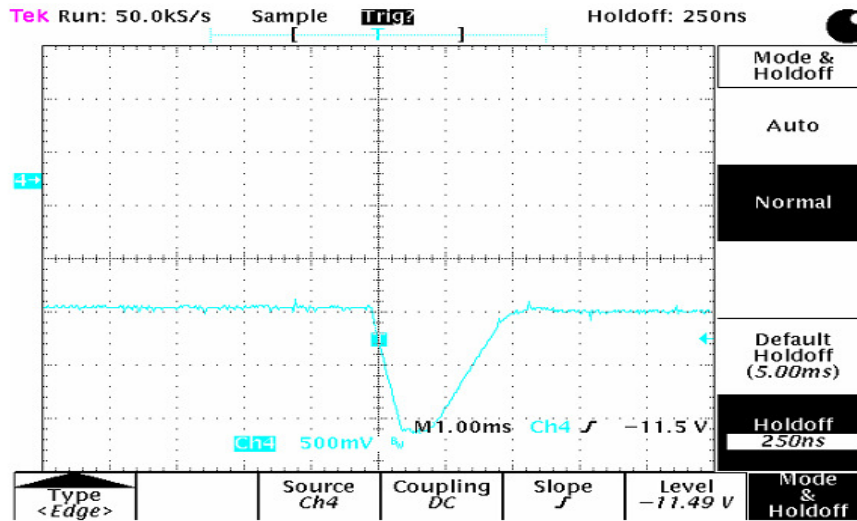


Figure.6. VOUT voltage overshoot from -12V to -13V upon sudden load change from 120mA to 10mA

In order to improve transient load behavior, a simple but effective solution has been found. To keep the regulation loop stable, a large compensation capacitor is required in CCM, but not in DCM. Therefore, the external big capacitor is disconnected in DCM. However, this is possible only if the external capacitor starts with the correct voltage immediately when entering CCM again. Best results have been achieved by making sure that the voltage across the external capacitor follows the internal much faster voltage signal all the time. Thus, switching back to CCM always starts with the correct operating point. Switching back to the large capacitor is a little bit delayed to allow the voltage to come up fast in case of a significant load step. Switches

as shown in figure 7 and a special low power output buffer are needed to improve transient load behavior. The ratio of the external capacitor to the internal capacitor can be 100 or even more.

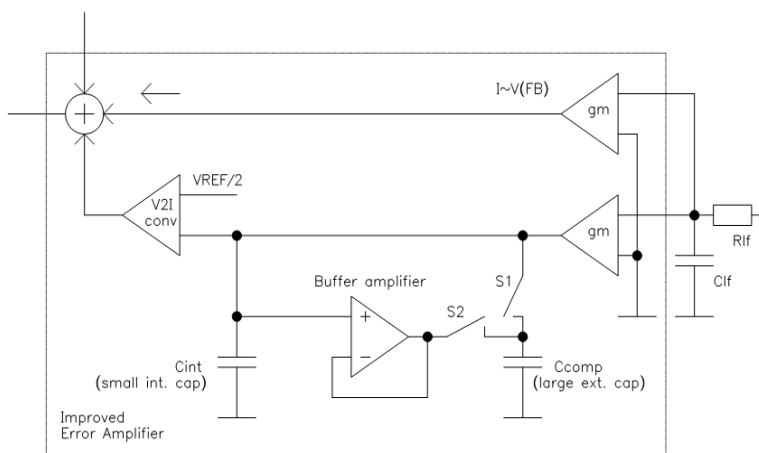


Figure.7. Transient load response improvement

The transient load response improvement reduces the output voltage drop from 2.5V to 0.6V as can be seen in figure 8. This means a 5% drop instead of 20%.

Also, the overshoot reduces significantly as can be seen in figure 9.

The transition point from CCM to DCM and vice versa can easily be detected by monitoring the SW pin. DCM means the inductor current becomes 0. Just before the current becomes 0, the voltage across the inductor is still VOUT. Since the voltage cannot jump to 0V immediately the current continues to flow for a moment and moves the voltage from VOUT to VIN before finally it can drop ringing to 0V. This first voltage jump can be detected easily as shown in figure 10.

A simple PMOS source follower provides the level shifting and due to capacitive coupling the propagation delay is only a few nanoseconds. An anti-series combination of two diodes protects the MOS devices from ESD strikes without clamping negative voltages too early.

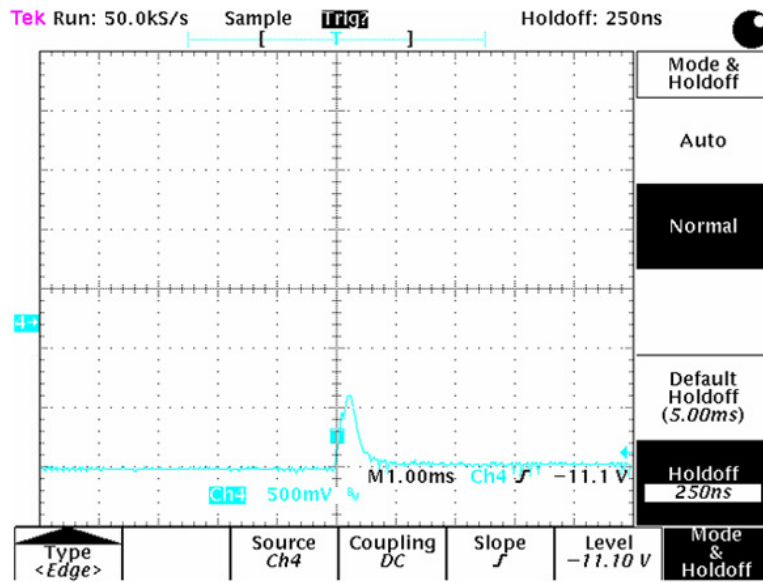


Figure.8. VOUT voltage drop from -12V to -11.4V upon sudden load change from 10mA to 120mA with transient load response improvement

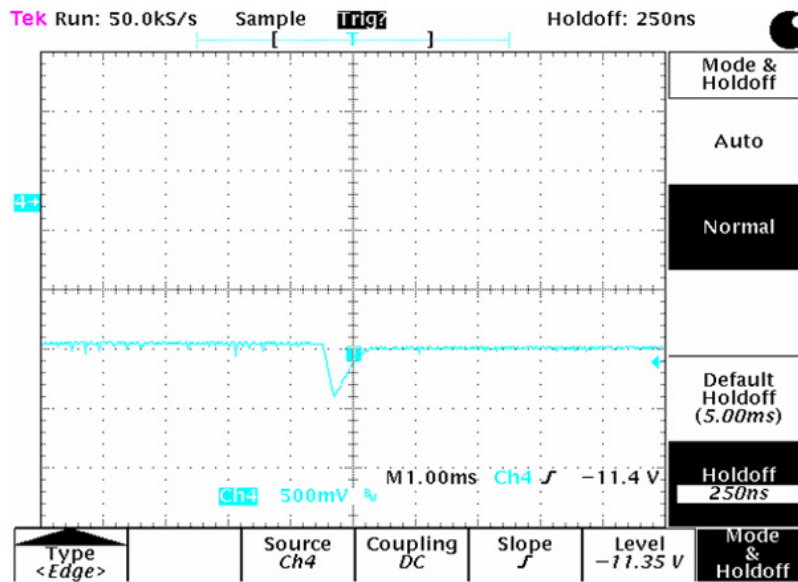


Figure.9. VOUT voltage overshoot from -12V to -12.4V upon sudden load change from 120mA to 10mA

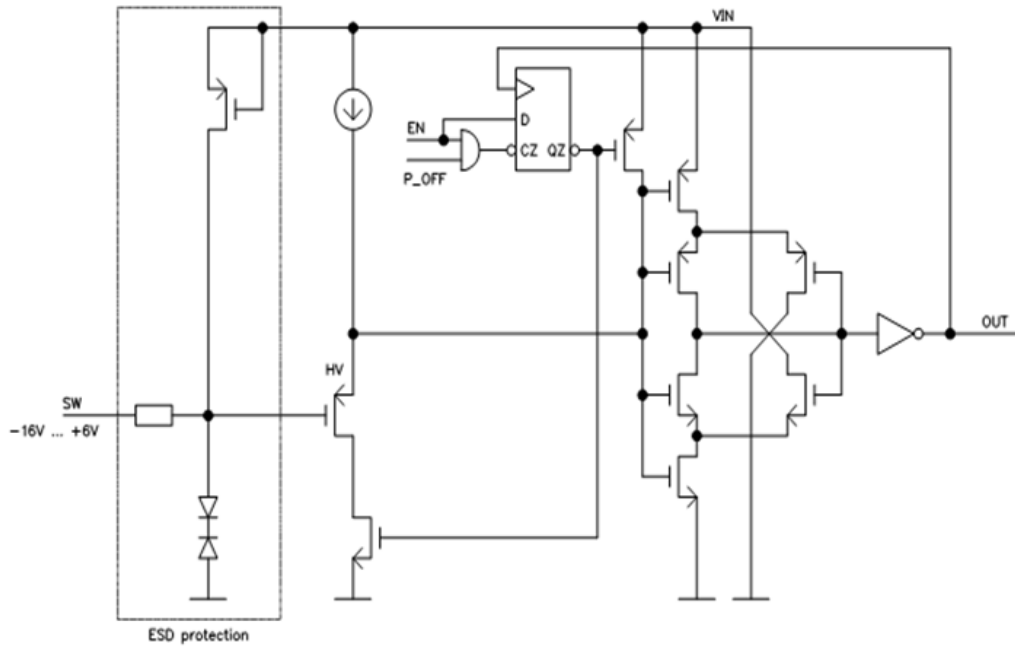


Figure.10.DCM / CCM detection

4. OVER-VOLTAGE PROTECTION

To protect external circuitry from negative voltages far above what can be tolerated, the circuit shown in figure 11 has been designed for solution where a separate comparator monitors the voltage feedback pin FB and stops switching whenever the output voltage exceeds the desired voltage by more than 10%. The additional second protection circuit directly monitors the negative output voltage. This makes sense for the case when the resistive voltage divider is broken. The output voltage limit has been set to -20V by choosing the resistor ratios accordingly.

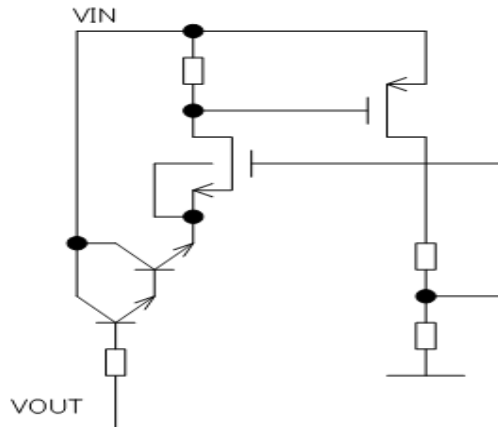


Figure .11. Over-voltage protection

5. FIXED VOLTAGE VERSIONS

Any output voltage from -2V to -15V can be generated by setting the appropriate values for the external voltage divider. Fixed voltage versions e.g. -5V, -12V and -15V do not need the external resistors. In contrast to converters that generate a positive output voltage, it is not possible to program various versions by using EEPROM bits. NMOS devices cannot be used to switch negative voltages without forward biased pn-junctions or they simply cannot be turned off. PMOS devices cannot be used to switch negative voltages without having an even more negative gate voltage applied. There is no practical solution. Therefore we decided to offer bond options that are easy to realize and do not add any new risks. Since copper bond pads can be placed over active area, there is no extra area consumption. Figure 12 shows the Fixed voltage versions by bond options

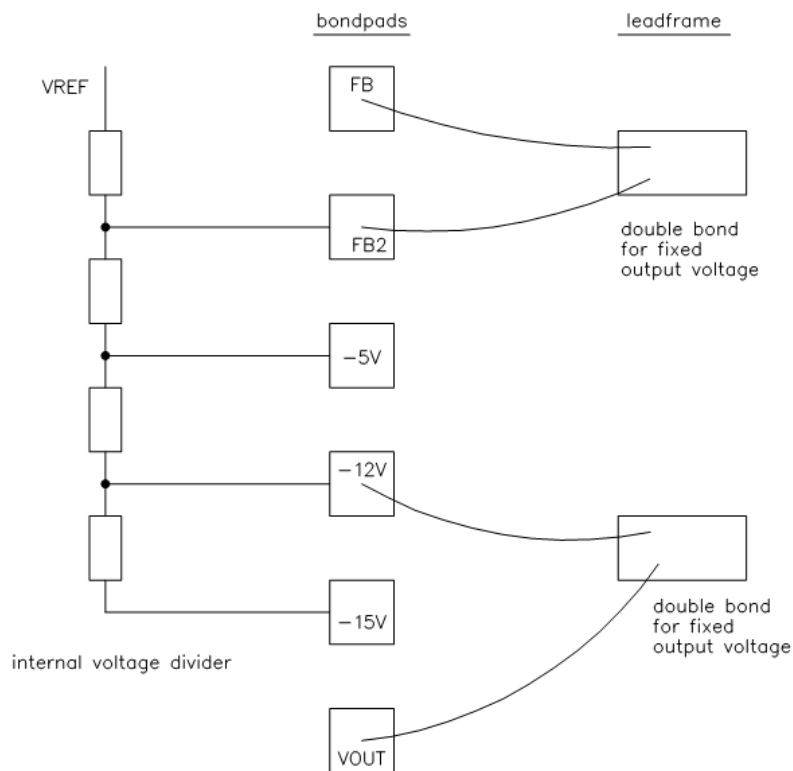


Figure .12. Fixed voltage versions by bond options

6. LAYOUT

The Layout of the proposed inverting buck-boost DCDC converter is shown in Figure. 13. Layout techniques such as guard rings and careful power and ground routing can minimize the spikes induced onto the sensitive linear sections.

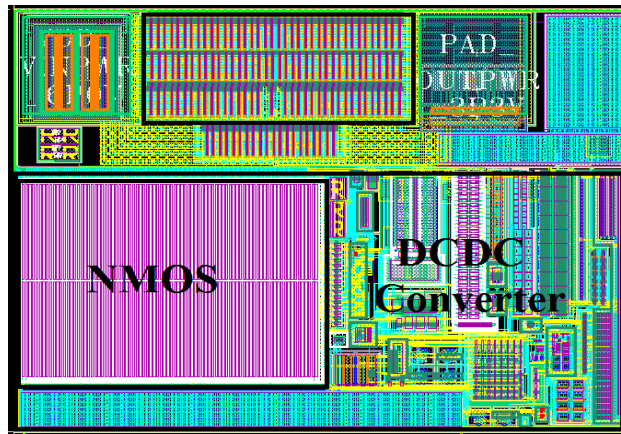


Figure.13. Layout of the proposed inverting buck-boost DCDC converter

7. CONCLUSION

The design of an inverting buck-boost DCDC converter design with a fixed-frequency PWM control topology for small digital camera or mobile phone displays has been presented. The proposed simple non-inverting buck-boost converter topology can be used successfully to generate negative supply voltages. Of course, using a diode instead of a switch costs efficiency, but we have achieved more than 80% in CCM which is 10% more than the competition device.

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