# FAST TRANSIENT RESPONSE LOW DROP-OUT VOLTAGE REGULATOR

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***ABSTRACT***

*This paper presents the design of Low Drop-Out (LDO) voltage regulator has fast transient response and which exploits a few current else low quiescent current in the operational amplifier PMOS type. We use band-gap reference for eliminate the temperature dependence. The proposed LDO voltage regulator implemented in 0.18-µm CMOS technology, we use Folded cascode CMOS amplifiers high performance in the stability , provide fast transient response which explains a fast settling, the LDO itself should provide in the output regulator voltages at $\Delta t$ equal 2ps with transient variation of the voltage less than 170mV. High accuracy in the DC response terms, the simulation results show that the accuracy of the output regulator voltages is 1.54±0.009V, and power consumption of 1.51 mW.*

***KEYWORDS***

*Low-dropout (LDO ) voltage regulator, Band-gap reference, Fast transient response, Current efficiency, Figure of merit & Layout.*

## 1.INTRODUCTION

The power management systems is importance and increased much in the electronics industry elsewhere the integrated circuits is exist in the last few years, The rationale is that LDO yields a good line and load regulation while maintaining a stable, constant and accuracy output voltage. Those battery-powered and handheld devices require advanced power management techniques to extend the life cycle of the battery and consequently the operation cycle of the device. I have chosen this architecture of a LDO linear regulator works for a frame made this set of specifications and find my position in the study of other integrated circuit with very high performance. All times power management in integrated circuits has been gaining a high-efficiency power management module is necessary such as low-power power converter or low dropout regulator to integrate circuit more attention because it allows for drastic reduction in the consumption of battery-powered portable equipment, such as cellular phones, pagers, laptops, camera recorders, and PDAs. The regulator is divided into two types, voltage mode LDO and current mode LDO, the regulator which uses the voltage mode is named linear regulator, therefore, the regulator which uses the current-mode is named shunt regulator. The power transistor of the voltage-mode linear regulator is series with the load resistant, an error amplifier and the power transistor are supplied by the same power supply (VIN), the series combination forms a voltage divider to reduce the unregulated input source to a regulated output one.

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This paper is organized as follows. In section II, description of circuit and the theoretical study of the characteristics proposed LDO voltage regulator are discussed. In section III, the static-state and dynamic-state characteristics are simulated and corresponding simulation results are summarized. The conclusion is derived in section IV.

## 2. LDO ARCHITECTURE

The top level structure of the proposed LDO shown in Fig. 1 It includes the following modules as error amplifier, band-gap reference, Equivalent Series Resistance (ESR), Power Transistor (PM) and Feedback Network (FN≡≡PD). This work presents a design of a LDO regulator in a 0.18-µm CMOS technology.

### 2.1. Description Of Circuit

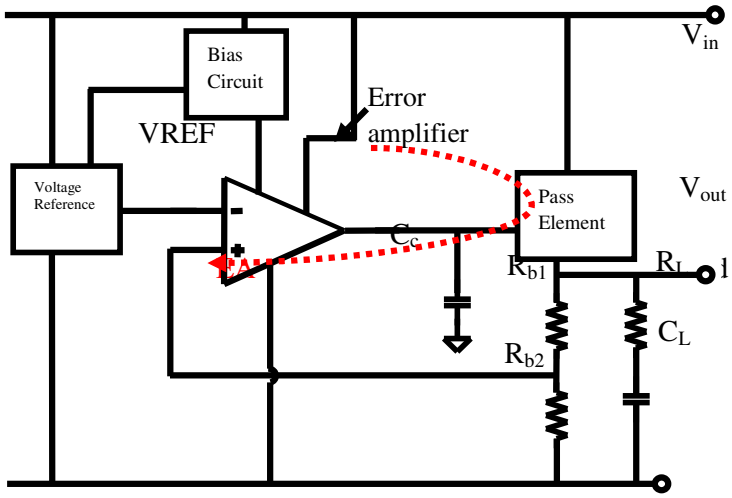


Fig. 1. Structure of the Regulator LDO Circuit.

The (Fig. 1) enclose a schematic of a regulators LDO voltage based on a PMOS, the structure of LDO implemented in CMOS 0.18µm technology. This transistor PMOS with common source connection as the pass element transistor between the input and output voltages. A part of the output voltage is fed back through R1 and R2 to the input of the amplifier and is compared to the voltage reference VREF. Capacitor CL stands for the capacitive load. The current Load (IL) represents the load whose current is supplied by the power transistor [1], [2], [4], [5].

An EA signal is fed back to the gate of the pass transistor through the feedback loop to respond to the load current while keeping the output voltage constant. The Voltage Control regulator which is an electrical regulator is designed to maintain a constant voltage level, the Voltage Control regulator regulates the Voltage supply to the load by adjusting the load current. It consists of an error amplifier, a power transistor, and the load elements.

## 2.2. Regulator Schematic And Parameters

The circuit of the proposed voltage -mode shunt regulator is shown in Fig. 2. Transistors M1 to M11 form the first-stage amplifier, while M12 to M1 form the bias amplifier. R1 and R2 are the resistive feedback network, the power transistor is labeled as MP. The error amplifier detects two input signal regarding the reference voltage VREF and the feedback signal Voltage between R1 and R2 . M32,M33 and M34 are the Simple current mirror in the band gap. from M22 to M31 form the two-stage operational amplifier utilized in this design is shown in Fig. 2, the band-gap circuit consists of two loops; one with negative feedback (through M23) and one with positive feedback (through M22), and since it consists of a nMOS differential pair operating, this may lead to stability especially if the positive feedback dominates over the negative feedback.

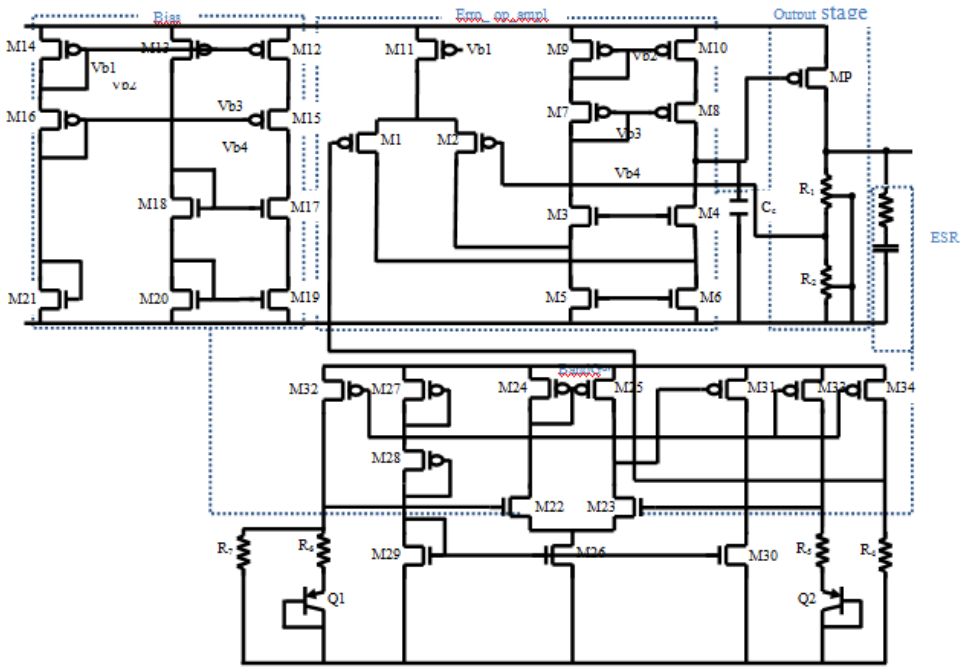


Fig. 2. Schematic of the proposed LDO voltage regulator.

From a equivalent small signal model of the proposed LDO. The small signal loop gain at low frequency can be given as bellow

$$G = A_{op\_amp} \times A_{MP}$$

Where

$$V_{sg} = V_s - V_g = V_{out} - V_{op\_amp}$$

$$R_{outop\_amp} = [(r_{ds7} + r_{ds9} + r_{ds7} r_{ds9} g_{m7}(1-\eta_7)) // r_{ds3}] + [(r_{ds1} // r_{ds5}) + r_{ds3}(r_{ds1} // r_{ds5}) g_{m3}(1+\eta_3)]$$

And

$$\begin{cases} A_{op\_amp} = g_{m1}[(r_{ds7} + r_{ds9} + r_{ds7} r_{ds9} g_{m7}(1-\eta_7))//r_{ds3}] + [(r_{ds1}//r_{ds5}) + r_{ds3}(r_{ds1}//r_{ds5}) g_{m3}(1+\eta_3)] \\ A_{MP} = g_{MP}\left(1/g_{dsP}//(R_1+R_2)\right)\left(R_1/R_1+R_2\right) \end{cases}$$

The dominant and non-dominant poles of the feedback loop can be given as

$$\begin{cases} C_1 = C_{gsMP} + \left[\left(C_{gdp8} + C_{gdp10}\right)//\left(C_{gdn4} + C_{gdn6}\right)\right] \\ C_2 = C_{gdMP} + C_c + C_{out\_op\_amp} \\ C_3 = C_{Load} \end{cases}$$

$$\begin{cases} f_1 = \dfrac{1}{2\pi R_{out\_op\_amp} C_c + C_{gdMP} + C_{out\_op\_amp}} \\ f_2 = \dfrac{1}{2\pi (g_{mMP}(r_{dsMP}//(R_1+R_2))C_L} \\ Z_0 = \dfrac{1}{2\pi (R_{ESR} C_L)} \end{cases}$$

### 2.2.1. Error Amplifier

The folded cascode operational amplifier (error amplifier) (EA) itself should provide very low power dissipation (especially in stand-by mode), and its bias currents must be kept as low as possible. It is apparent that a speed/dissipation trade-off arises, and the main limitation is manifested in terms of slew-rate of the error amplifier.

As an example, if the EA can deliver to a 5-pF power-MOS gate no more than 2μA of current, producing a 1.54 -V step will take 2ps of slewing interval. This allows improvement to the transient response without increasing the DC consumption.

Considering that during this time the control loop of the LDO is interrupted and that the output voltage is out of control, it is apparent that such a long slewing period may negatively impact on the LDO performance, especially in terms of output voltage overshoots which may become unacceptable for many applications.

### 2.2.2. Band-Gap

A CMOS band-gap reference circuit shown in Fig. 2 operates in a current-mode. A temperature independent current is first generated by summing the proportional to absolute temperature (PTAT) current IR7 and the complementary to absolute temperature (CTAT) current IR6. Assuming M32, M33 and M34 have the same size [4],[5], the proposed band-gap reference uses the Simple current mirror to decrease the surface layout of the Band-gap.

$I = I_1 + I_2$

And yet

$$\begin{cases} V^+ = V_A = R_5\ I_1 + V_{be1} \\ V^- = V_B = V_{be1} = R_6\ I_2 \end{cases}$$

Then

$V^+ \approx V^-$ Else $R_5\ I_1 + V_{be1} = V_{be2}$

So he said to

$$I_1 = \frac{V_{be2} - V_{be1}}{R_2} = \frac{\Delta V_{be}}{R_2}$$

$$\Delta V_{be} = V_t \ln(n)$$

$$\begin{cases} I_1 = \dfrac{V_t \ln(n)}{R_5} \\ I_2 = \dfrac{V_{be2}}{R_6} \end{cases}$$

Then $$V_{REF} = R_4 \left( \frac{V_t \ln(n)}{R_5} + \frac{V_{be2}}{R_6} \right)$$

## 3. Simulated And Experimental Results

The LDO Circuit has been implemented in 0.18-$\mu$m CMOS technology. This work is improved by the use of CMOs capacity (CT) so the advantage of reducing the area in the Layout is shown in (Fig. 3) in which the effective die area is $10.853 \times 10^{-3}$ mm$^2$

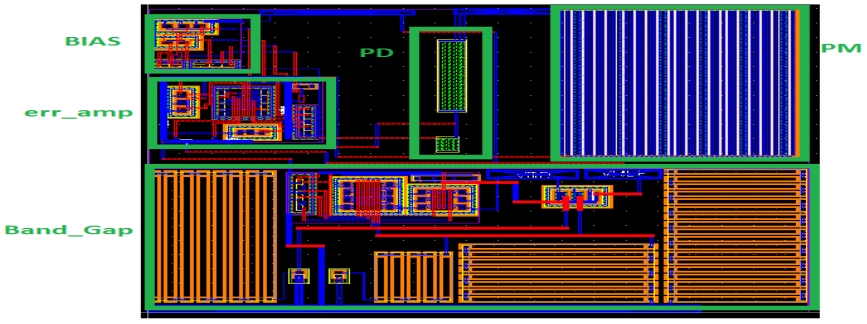


Fig. 3. Layout of this work (LDO).

For testing the LDO and external current mirror was used, and its output impedance is heavily dependent of the amount of current. The LDO regulator is tested for R1 =0.5 kΩ, R2 = 1.5 kΩ ,VDD = 1.8 V, VREF = 1.2 V and multilayer ceramic output CMOS capacitor 500 pF with several bypass CMOS capacitors in the f F range placed in parallel to reduce high-frequency noise. The dc output voltage of the regulator is 1.54V. The ground current consumed by the LDO regulator is 52 µA.

### 3.1. Gain , Phase And Stability Considerations

From the simulation results in Fig.4, the proposed LDO regulator is stable for load current values ranging from 0 to 50 mA with a gain of the pass band is 85 dB. The phase margin is better than 60° for all cases then the LDO with the compensation is stable showing that the phase margin is good enough.


Fig. 4 : Frequency response of the proposed LOO

### 3.2. Static-State Regulation Characteristics

The current mass is the sum of all currents polarization including in the regulator: the current feedback, the current error amplifier and the drive current of the power transistor [2], [7].The current mass is 52µA. The simulation results of different corners are as follows: The characteristic of input voltage (Vin) and the output voltage (Vout) for our LDO voltage regulator shown in Fig. 5. The drop-out voltage is 260 mV. The DC line regulation is 0.642%. The output voltage of the proposed LDO voltage regulator with the load current swept from 100µA to 50mA is given in Fig.6 the load regulation is $0.18x10^{-3}$ mV/mA. The current efficiency is 99.8% and the power efficiency is 86%. The figure of merit (FOM) is 2.8ps.

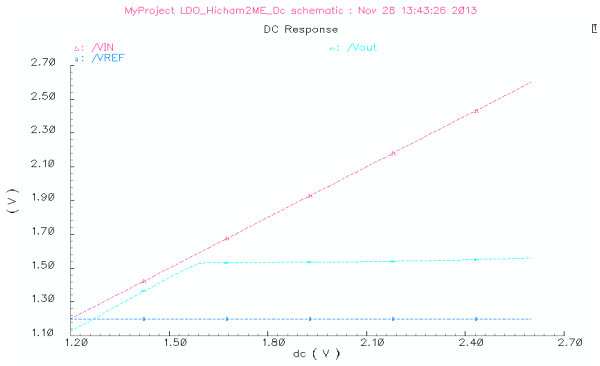


Fig. 5. The DC sweep of the LDO

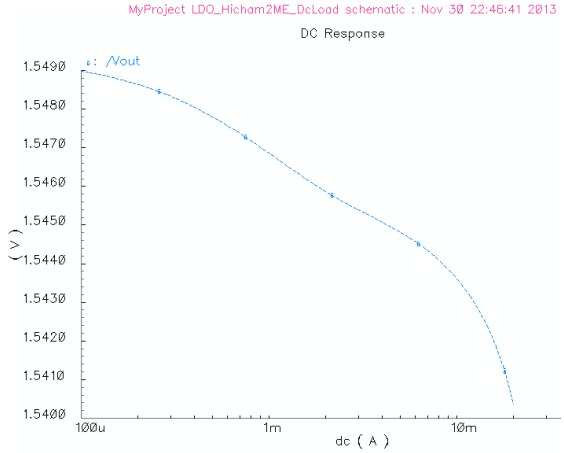


Fig. 6. DC Load regulation of the LDO.

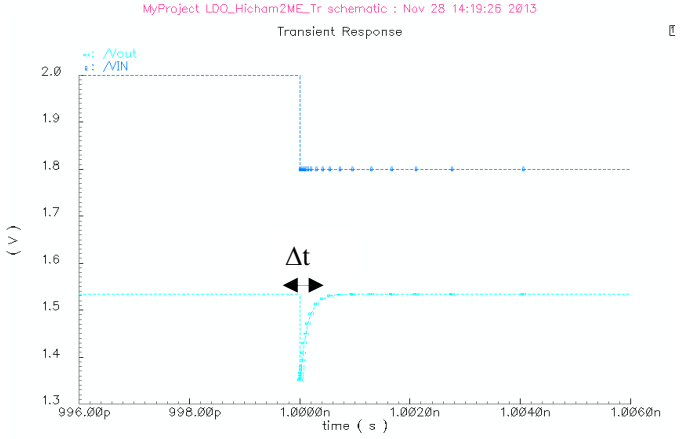


Fig.7. Transient output voltage of the LDO regulator.

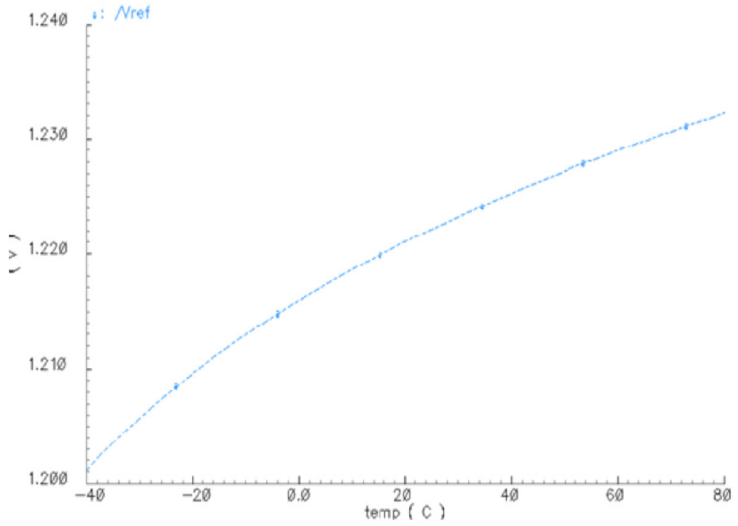


Fig.8. Simulated Temperature Variation of the proposed bandgap reference circuit shown in Fig2.

The simulation results of the transient response shown in Fig.8. The transient response increases further with different voltage input VIN from 2 V to 1.8 V and increasing the capacity CL, if $\Delta t$ = 2ps so he said to fast transient response [2],[3], [8]. Fig. 9 shows the simulated temperature variation of the generated bias voltage 1.2 V that has a 30 mV variation in a temperature range of -40°C to 80 °C .

## 4. CONCLUSIONS

LDO dropout is minimized to guarantee high power supply rejection at optimized efficiency. In the meanwhile, current efficiency is enhanced up to 99.8 % because of low quiescent current operation. The design procedure for obtaining the proper accuracy in the DC response low quiescent current and fast transient output for to integrate with other circuit, involving a high result of the figure of merit equal 2ps. Table I provides a performance comparison between this work and recently published designs.

Table 1. Performance summary and comparison.

| Parameter | [1] | [2] | [3] | [6] | This Work |
|---|---|---|---|---|---|
| Technology (µm) | 0. 18 µm | 0.11µm | 0.18 µm | 0. 18 µm | 0. 18 µm |
| Drop out voltage (mV) | 300 | 385 | 200 | 190 | 260 |
| Ground Current (IQ) | 28µA | 41.5µA | 40 µA | 120µA | 52 µA |
| Band-gap included | YES | NO | NO | NO | YES |
| Settling time | 1.6 µs | 77ps | 1.172µs/ 1.055 µs | 1400ns/ 1100ns | 2ps |
| Active Area | 104400 mm2 | 210000 µm2 | 43940 µm2 | - | 10853 µm2 |

## REFERENCES


[1] Vahid Majidzadeh, Alexandre Schmid, and YusufLeblebici, " A Fully On-Chip LDO Voltage Regulator for Remotely Powered Cortical Implants ", IEEE Transactions 978-1-4244-4353-6 /09 /$25 .00 ©2 0 0 9 IEEE.

[2] Young-il Kim and Sang-sun Lee, " A Capacitorless LDO Regulator With Fast Feedback Technique and Low-Quiescent Current Error Amplifier", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 60, NO. 6, JUNE 2013.

[3] Cheekala Lovaraju, Ashis Maity, and Amit Patra, " A Capacitor-less Low Drop-out (LDO) Regulator with Improved Transient Response for System-on-Chip Applications", 2013 26th International Conference on VLSI Design and the 12th International Conference on Embedded Systems.

[4] Andrea Boni, Member, IEEE, "Op-Amps and Startup Circuits for CMOS Bandgap References" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL 37, NO. 10, OCTOBER 2002.

[5] Chia-Chun Tsai, Tsung-Ming Liu, and Trong-Yen Lee "Micro Fuel Cell Power Management Circuit Design for Portable Devices" 2012 9th International Conference on Fuzzy Systems and Knowledge Discovery (FSKD 2012).

[6] J.H.Wang,C.H.Tsai, and S. W.Lai, "A low-dropout regulator with tail current control for DPWM clock correction"IEEE Trans. Circuits Syst. II, Exp.Briefs,vol. 59, no.1, pp.4549, Jan. 2012.

[7] Dongpo Chen, Lenian He and Xiaolang Yan, "A Low-dropout Regulator with Unconditional Stability and Low Quiescent Current", IEEE Transactions on Power electronics, 0-7803-9584-0/06/$20.00O2006 IEEE.

[8] W. Chen, W.H. Ki, and P.K.T. Mok, "Dual-Loop Feedback for Fast Low Dropout Regulators," Proc. IEEE PESC, vol. 3, Jun.2001, pp.1265-1269.

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