HIGH PERFORMANCE ETHERNET PACKET PROCESSOR CORE FOR NEXT GENERATION NETWORKS

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ABSTRACT

As the demand for high speed Internet significantly increasing to meet the requirement of large data transfers, real-time communication and High Definition (HD) multimedia transfer over IP, the IP based network products architecture must evolve and change. Application specific processors require high performance, low power and high degree of programmability is the limitation in many general processor based applications. This paper describes the design of Ethernet packet processor for system-on-chip (SoC) which performs all core packet processing functions, including segmentation and reassembly, packetization classification, route and queue management which will speedup switching/routing performance making it more suitable for Next Generation Networks (NGN). Ethernet packet processor design can be configured for use with multiple projects targeted to a FPGA device the system is designed to support 1/10/20/40/100 Gigabit links with a speed and performance advantage. VHDL has been used to implement and simulated the required functions in FPGA.

KEYWORDS

Ethernet, SoC, FPGA, NGN, LAN Router and Switches, IP networks, 1/10/20/40/100 Gigabit.

1. INTRODUCTION

With the advancements in networking technology, most networks converge on Ethernet and IP as the dominant transport technology and the ability to manage and process the IP packets at high speed is a key to offering successful new services. There are different speeds 1/10/20/40/100 Gigabit with electrical and optical interfaces available in modern networks. Packet processors intercept individual IP data packets and to process them using hardware solution which can be easily enhanced to add new capabilities. In the next generation network high speed packet processing is critical for low-latency applications such as multimedia and Voice over IP (VoIP). Multicore packet processing building blocks are found in SoC based Ethernet Packet Processor to meet the high performance. Next Generation Networks (NGN) need to be designed for high performance requirements.

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Data encapsulation process includes frame assembly before transmission and frame decoding upon reception of a frame. While encoding the frame MAC layer adds a header and trailer to the layer 3 payload. The use of frames in the transmission of bits as they are placed on the media and in the grouping of bits at the receiving node. Frame encode process provides important delimiters that are used to identify a group of bits that make up a frame. This process provides synchronization between the transmitting and receiving nodes. Encapsulation process also provides for Data Link layer addressing. Each Ethernet header added in the frame contains the physical MAC address that enables a frame to be delivered to a destination node. Also function of data encapsulation is error detection. Each Ethernet frame contains a trailer with a cyclic redundancy check (CRC) of the frame contents. After reception of a frame, the receiving node creates a CRC to compare to the one in the frame. If these two CRC calculations match and the frame can be trusted to have been received without error.

The Ethernet packet processor handles following fields:

Preamble (PR): seven bytes. it is an alternating pattern of ones and zeros that tells receiving stations that a frame is coming, and that provides a means to synchronize the frame-reception portions of receiving physical layers with the incoming bit stream.
Start-of-frame delimiter (SFD): one byte. The SOF (start of frame) is an alternating pattern of ones and zeros, ending with two consecutive 1-bits indicating that the next bit is the left-most bit in the left-most byte of the destination address.
Destination address (DA): one bytes. The DA field identifies which station should receive the frame.
Source addresses (SA): one bytes. The SA field identifies the sending station.
Length Type: it is two bytes. This field indicates either the number of MAC- data bytes that are contained in the data field of the frame, or the frame type ID if the frame is assembled using an optional format.
Data- it is a sequence of bytes from 46 to 1500 of any value. Minimum frame size is 64bytes.
Cyclic redundancy check (CRC) - 4 bytes. This sequence contains a 32-bit cyclic redundancy check (CRC) value, which is created by the sending MAC and is recalculated by the receiving MAC to check for damaged frames. The packet format is as shown in Figure 1 and decoding of Ethernet Frame is shown in Figure 2.

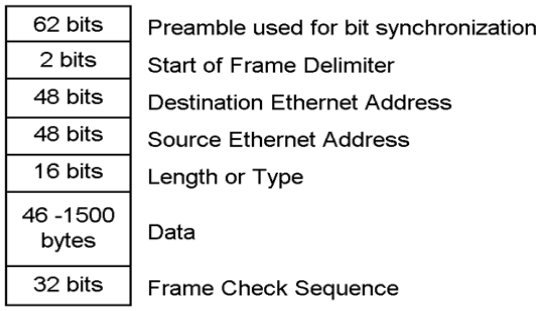

Figure1.Ethernet Frame Format

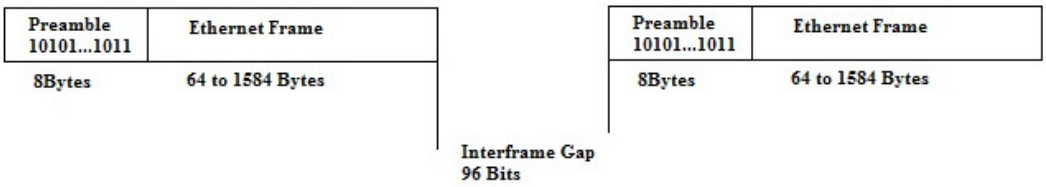

Figure 2. Decoding Ethernet Frame

1.1 SYSTEM ON CHIP (SoC)

System on chip (SoC or SOC) refers to integrating many functional or peripherals of a embedded system or other electronic system into a single integrated circuit . It may contain digital, analog, mixed-signal, and often radio-frequency functions - all on a single chip substrate. A typical application is in the area of embedded systems. The contrast with a microcontroller is one of degree. Microcontrollers typically have multi functional blocks each block perform specific function and are single-chip-systems; whereas the term SoC is typically used with more powerful processors, capable of running software such as embedded OS like UCLinux, which need external memory chips like DDR, FLASH and which are used with various external peripherals increasing chip integration to reduce manufacturing costs, power and smaller systems. Application specific processors are too complex to fit on just one chip built with a process optimized for just one of the application tasks.

A SoC consists of both the hardware and the software that controls the microcontroller, microprocessor or DSP cores, peripherals and interfaces. Most SoCs are developed from pre-qualified hardware blocks for the hardware elements described above, together with the software drivers that control their operation. The hardware blocks are put together using EDA tools; the software modules are integrated using a software development environment. A key step in the design flow is emulation: the hardware is mapped onto an emulation platform based on a field programmable gate array (FPGA) that mimics the behavior of the SoC, and the software modules are loaded into the memory of the emulation platform. SoC the emulation platform enables the hardware and software of the SoC to be tested and debugged at close to its full operational speed. After emulation the hardware of the SoC follows the place and route phase of the design of an integrated circuit before it is fabricated.

In this paper Ethernet packet processor core is developed to use in SoC application for design of high performance switches, router and other IP based products for next generation networks (NGN). Ethernet packet processor code acts as hardware accelerator for processing packets in SoC.

1.2 OUR CONTRIBUTIONS

In this paper, we provide the design and implementation aspects of Ethernet packet processors for new generation IP Network technology, which is designed to address the performance and flexibility problems of new generation IP products (1/10/20/40/100 Gigabit).we proposed to use

Ethernet packet processor for next generation internet protocol based products to meet high performance requirements by providing hardware acceleration for frequently handled functions in packet processing. The usage Ethernet packet processor (EPP) in design and development of multiport switches and router is also discussed.

2. LITERARURE SURVEY

General purpose processors cannot provide wire speed performance for Packet processing and analysis. Embedded ASIC hardware has extremely high cost and is difficult to implement and requires many months of fabricate a chip for even small changes. The embedded processor can handle only specified functionality with limited wire speed performance. Packet processing needs balance between the architecture and network flow. Developing Real time packet Analysis which can receive the packets processes the packets and forwards the packet with wire speed while utilizing the maximum network bandwidth as well as to marinating security in the network is an ideal application. Network traffic analysis includes capturing of data from network and inspecting of data at each layer. The exponential growth of Internet traffic, network bandwidth and Internet based applications rise problems of performance, flexibility in network traffic analysis. Flexibility achieved through the programmable devices like General purpose processors and performance can achieve through hardwired solutions like Field Programmable Gate Arrays. Implementation comparison is shown in Figure 2.1 [23].

Network processors and field-programmable gate arrays (FPGAs) offer an interesting middle ground. Network processors are CPUs tuned for performing networking tasks. While they are sometimes faster for very specific tasks, they achieve that speed by optimizing for a very specific task: network processing. It's very easy to push a network processor outside the design target by adding new functionality. The network processor is often slower than a general-purpose processor performing the same task. Network processors often have very low clock speeds.. Finally, the costs for network processors is often on-par or even more expensive than a general-purpose CPU, since volumes are smaller and the market more specialized. With General purpose processors we can’t achieve wire speed performance; with FPGA technology Network processors are new generation technology, which is designed to address the performance and flexibility problems. Network processors, analyzes Lower level layers by hardware and higher level layer by software with parallel and pipelined architecture. With multiple micro engines and with parallel and pipelining programming architecture network processors makes network processing at wire speed [18][19][20][21][22].

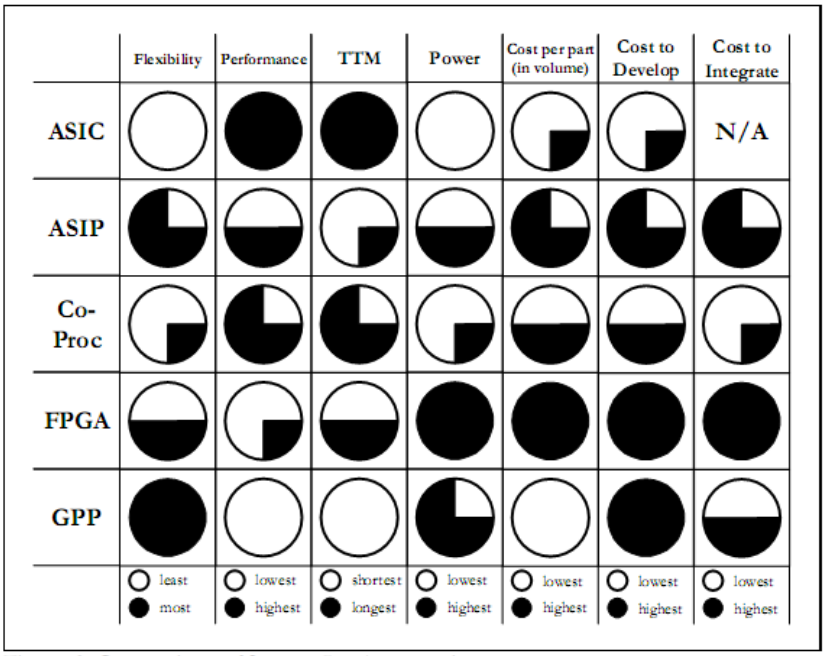

Figure 2.1 Implementation Comparison Courtesy [23]

The features of Ethernet packet Processors (EPP) are compared from the following perspectives.

Performance - by multiple parallel EPPs in SoC, EPPs are able to perform many applications at wire speed.
Flexibility – having hardware IP (intellectual properties) core as a major part of the system allows network equipment to easily adapt to changing standards and applications
Fast TTM – reuse of ready EPP core is much faster (and cheaper) than designing hardware and software of equivalent functionality
Power – while EPPs are optimized for low power consumption and area, their power consumption is important for cost reasons (e.g. implications on packaging).

Major goal of the designing EPP is that may include functionality, performance, power consumption and manufacturing cost. Performance means the processing speed of the product, which may be a combination of soft deadlines such as approximate time to perform a user-level function and hard deadlines by which a particular operation must be completed. Since EPP uses parallel blocks, the single clock is used for these blocks to perform individual requirements; the power consumption is brought down. And manufacturing cost primarily defines the cost of the hardware components.

Performance and flexibility. Traditional network processing mainly focuses on forwarding packet at high speed in order to eliminate the network bottlenecks. Network devices are expected to perform at high speed with low latency. However, as the Internet Protocol keeps maturing, newer protocols have been emerging and will emerge in the future. Such newer protocols include

IPv6, security, signaling, and various network managements, etc. Ethernet packet processors are also expected to flexibly support these newer protocols and applications with high performance.

3. PROPOSED ARCHITECTURE AND DESIGN METHODOLOGY

Those general purpose processors based architecture suffers from very low performance that hinder them from being suitable for many applications such as L2/L3 switches, routers and Gigabit routers. Because of architectural constraints and number of clocks requirement for executing instructions to perform functions application specific processors are not suitable for high performance and low power requirements, however Ethernet packet processor allow much faster packet processing capability by using multi functional parallel processing blocks. Each individual blocks in the Ethernet packet processor receives data at MII, RMII, GMII etc interface parallel data and perform specific functions like extraction and encapsulation of SFD, source or destination MAC ID,L2,L3, CRC calculation and IFG.

The potential solution is to make use of the Field Programmable Gate Arrays (FPGAs), have introduced a great deal of speed and flexibility and performance into machine fast controls and operations. Ethernet is a popular protocol choice in FPGAs because of its flexibility, reliability, and performance they are extensively used to implement highly specialized tasks where simplicity, low production cost, and reliability are big assets. Even if simple and reliable, these systems need means for communications.

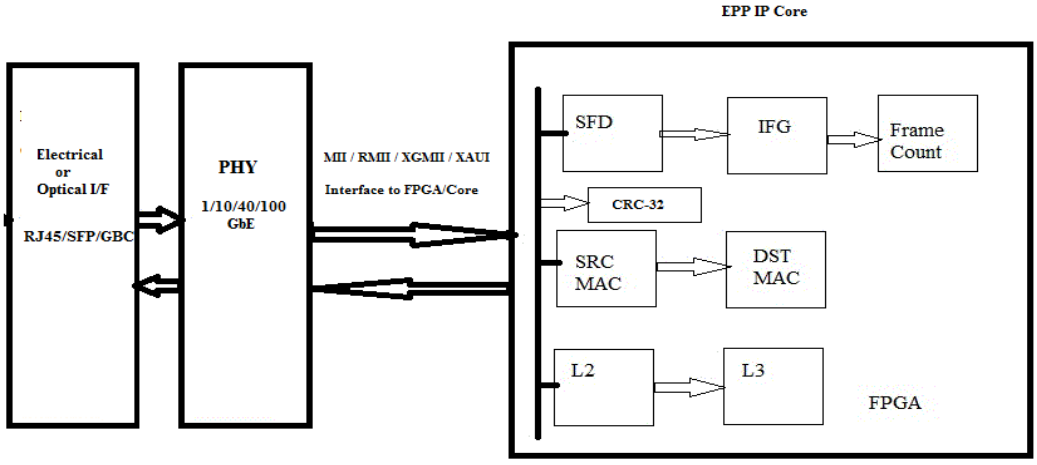

Figure 3. Ethernet Packet Processor

An outline of the proposed architecture design is shown in Figure 3. Main components are Ethernet packet Processor, 1/10/20/40/100 Gigabit interface Connector. Ethernet Packet Processor consists of six VHDL Modules. The core functionality is implemented in the Aggregate module, which has been custom-designed using VHDL. Such as detection of SFD, source MAC, destination MAC, payload length and CRC detection/calculation. A clean separation between these module and rest of the design allows for flexibility and portability, benefiting from well defined independent interfaces. Networking cores provides fertile ground for designing highly modular and re-usable components. Packet processing in FPGA is done by a chain of dedicated pipelined blocks. We implemented programmable synchronous pipeline arrays of individual

block for high performance. The multi functional blocks integrated into single chip is called System on Chip (SoC).

The Ethernet Packet Processor analyzes the receiving frame. The packet is received and decoded to all individual sub entity of the packet. It identifies the type of Ethernet encapsulation, type of protocol, and extracts the fields in the packet needed by the Address look-up. The Packet processor performs start of frame preamble (SFD), inter frame gap (IFG) detection, and Packet length count, source. Destination MAC address and Layer2/Layer3/Layer4 parsing to extract information from the headers of these three layers. Therefore, protocols of these three layers have to be considered. The CRC calculation is done to check integrity of transmitted and received frame. The identification of SFD and calculation/detection of CRC is found to be time and memory consuming task in all IP based products. In this design we proposed hardware acceleration of these tasks to offload processor tasks. Similarly source and destination MAC address, IP address extraction and Frame length count is important tasks in switching and routing, EPP provides pipelined blocks to meet these task to improve performance of next generation IP products.

Most of the modern communication protocols use some error detection algorithms. Cyclic Redundancy Check, or CRC, is the most popular one among these. CRC properties are defined by the generator polynomial length and coefficients. The protocol specification usually defines CRC in hex or polynomial notation. Cyclic redundancy check has major role in deciding performance of system, which is carried repeatedly whenever frame is transmitted and received. The Cyclic Redundancy Check can be used as a checksum to detect the accidental alteration of data during transmission or storage. It is used in Ethernet packets to verify the content and detect errors. CRC-32 block is implemented to meet high performance requirement. It is most optimized CRC-32 block in Ethernet packet processor, the core accepts data packets with packet start and stop aligned to any octet boundary. This functional block of CRC-32 generation and checking at high speed uses an efficient pipelined CRC calculation algorithm. Cyclic redundancy check algorithm is derived from the mathematics of polynomial division modulo two, as result the code seen in practice deviates confusingly from 'pure' division and the register may shift left or right. Another CRC that is other than CRC-8 or CRC-16 is the ubiquitous 32-bit *CRC-32*, which is used in Ethernet. The CRC-32 polynomial is x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 +x2 + x + 1 and its LFSR implementation is shown in Figure 3a.

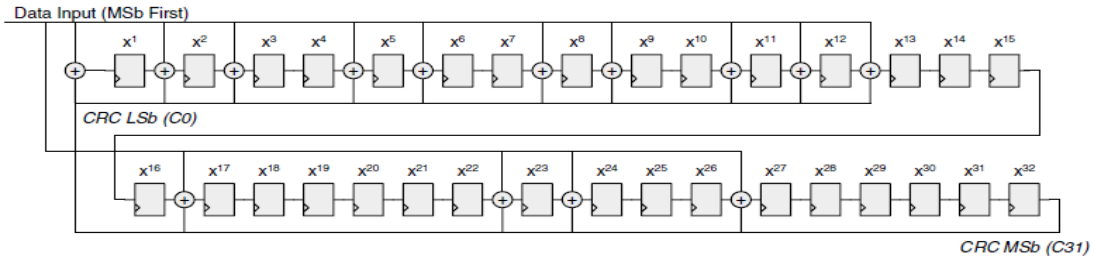

Figure 3a. Procedure for CRC-32

3.1 PROOF OF CONCEPT AND APPLICATIONS

EPP play role of hardware acceleration in design of new generation IP products for achieving high performance. The two simple examples of usage of EPP in design of switches and routers are discussed.

3.1.1 LAN Switch Design Using Ethernet Packet Processor

Ethernet switch connects multiple Ethernet LAN ports. Each port on the switch can be connected to a different LAN port; this topology forms a larger Ethernet network. Ethernet switch is used to interconnect a number of Ethernet local area networks (LANs) to form a large Ethernet network as shown in Figure4. The switch stores the media access controller (MAC) address in buffer which is extracted from frames received through each port to identify each network segment. MAC address are used to switch forward frames from the source port to the destination sport instead of forwarding the frame to all the connected ports, hence consequently reducing network traffic. If packet has CRC error, packets are discarded. Otherwise, the switch looks up the MAC address and sends the packet on to the destination node. Many switches combine the two methods by using cut-through until a certain error level is reached, then changing over to store and forward. Few switches are strictly cut-through because this provides no error correction [2] [3] [4].

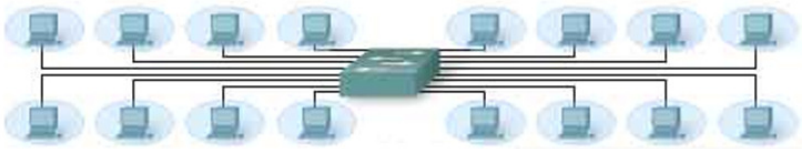

Figure4: LAN network using Ethernet Switch.

Since processor based switch design is busy in collecting information required for switching and switching between port lead to latency. Application specific solutions for multi-port Ethernet switches are widely available from different vendors and can be used to meet the switching requirements of a number of applications. However these do not provide a good solution for applications that require high performance features and such as a configuration of an odd number of ports or a configuration of ports of varying speeds. Multiple latencies resulting from this scheme could improve the overall performance when combined with Ethernet Packet Processor in SoC is shown Figure 4a.

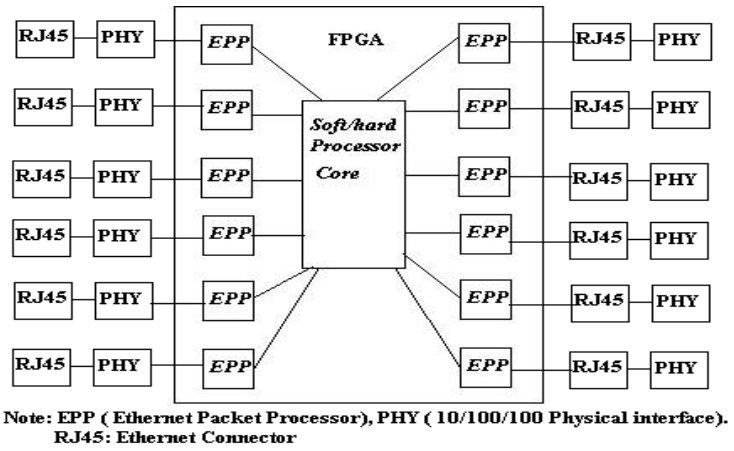

Figure 4a: High capacity LAN Switch Architecture.

3.1.2 Router Design Using Ethernet Packet Processor

The present networks routers have traditionally been implemented purely in software using ASIC processors. Because of the software implementation, the performance of a router was limited by the performance of the ASIC processor executing the protocol code. To achieve wire-speed routing, high-performance processors together with hardware logic were required. This translated into higher cost and area

Next Generation IP Routers require multi gigabit (1/10/20/40/100/1000G) networking technologies where IP routers will be used to interconnect backbone networks. Routers also to act as points of attachments to high performance WAN links [1]. New generation network routers require powerful architectures to meet high performance bandwidth requirements.. Therefore, the design of high speed IP routers has been a major area of research. New generation optical networking technologies are pushing link rates in high speed IP routers beyond 10G and 40 Gbps. Such high rates demand that packet forwarding in IP routers must be performed in hardware. The FPGA based cores are reconfigured to take into account changes in the bandwidth demands and routing characteristics [15]. While the FPGA is being reconfigured, all traffic is routed by the hardware logic. When reconfiguration is finished, selected virtual networks are shifted back to the hardware based on their performance requirements.

Next Generation IP routers require multi gigabit (1/10/20/40/100Gigabit) networking technologies .The Packets are received at router input and router will open the packet, decode the Ethernet frame, finds the ultimate destination address and encode the packet, giving it a new IP header that will send it to next hop. The router checks IP address at the Network layer, source and destination addresses to determine the path for the packet transportation over the network. Router carries layer 3 networking activity.

The evolution of IP router designs and highlights the major performance issues affecting IP routers. The need to build fast IP routers is being studied in a variety of ways. Our literature

survey summarizes that various router blocks and their mechanism needed for improving high speed performance operation and architectural constraints imposed by the various router design alternatives of routers in present networks. Avoiding centralized processor route lookups, and administration, is the requirements of new generation router design, router hardware can be made more reliable by adding Ethernet packet processor could be one method for fast packet processing. One of proposed router architecture using Ethernet packet processor is shown in figure5 for various LAN and WAN interfaces.

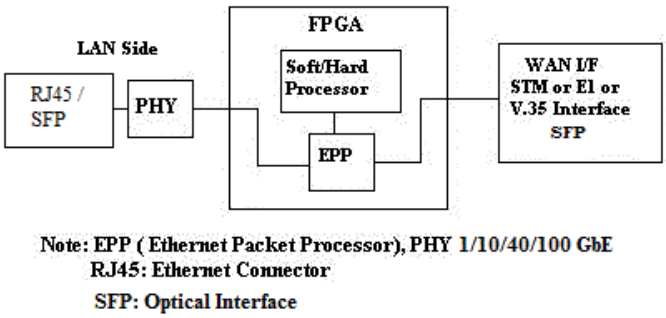

Figure 5: High Speed high performance Router Design

4. CONCLUSIONS

A novel design methodology to design a internet protocol specific packet processor has been introduced to have hardware acceleration for process and pass packets at high speed 1/10/20/40/100 Gigabit. We have designed an interface that directly translates the way packets need to be processed into a simple clean pipeline that has enough flexibility to allow for designing some powerful extensions to a basic switches and routers. Using this methodology, a very compact domain specific SoC can be designed using Ethernet packet processing core while maintaining the high speed requirements of Ethernet/IP switches and router. This Method finds wide application in design of Ethernet based products including high performance high capacity L2/L3 switches and router at 1/10/40/100 Gigabit is possible with this method.

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