IMPLEMENTATION OF PIPELINED ARCHITECTURE FOR PHYSICAL DOWNLINK CHANNELS OF 3GPP-LTE

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ABSTRACT

LTE (Long Term Evolution) is a high data rate, low latency and packet optimized radio access technology designed to support roaming Internet access via cell phones and handheld devices in 3G and 4G networks. This paper mainly focuses on to improve the processing speed and decrease the maximum delay of the downlink channels using the pipelined buffer controlled technique. This paper proposes Pipelined buffer controlled Architecture for both transmitter and receiver for Physical Downlink channels of 3GPP-LTE. The transmitter architecture comprises Bit Scrambling, Modulation mapping, Layer mapping, Precoding and Resource element mapping modules. The receiver architecture comprises Demapping from resource elements, Decoding, Comparing and Detection, Delayer mapping and Descrambling modules as described in LTE specifications. In addition to these, buffers are included in both transmitter and receiver architectures. Modelsim is used for simulation, synthesis and implementation are achieved using PlanAhead13.2 tool on Virtex-5, xc5vlx50tff1136-1 device board is used. Implemented results are discussed in terms of RTL design, FPGA editor, Power estimation and Resource estimation.

KEYWORDS

LTE, SISO, MISO, MIMO, PBCH, PDSCH, PCFICH, PHICH, PDCCH, PMCH

1. INTRODUCTION

The Long Term Evolution of UMTS (Universal Mobile Telecommunication Systems) is one of the recent advancements in today's mobile telecommunications systems. Though GSM technology has improved in a certain manner by connecting communities and individuals in remote regions where fixed-line connectivity was nonexistent, the successor of GSM, developed by the 3GPP (Third Generation Partnership Projects) LTE is framed to increase the speed and capacity of voice as well as data signals. There are many issues relating to the implementation of LTE. The hardware architecture in the physical layer is one of the key research topics for the VLSI Engineers. The main objective of this paper is to bring the pipelined buffer controlled architecture of downlink data and control channels for transmitter and receiver.

DOI : 10.5121/ijngn.2013.5101

There are two types of radio frame structures for LTE: Type-1 frame structure is applicable to Frequency Division Duplex and type-2 frame structure is related to Time Division Duplex. This paper is framed for type 1 Frame structure which is shown in Figure 1. Each radio frame is $T_f = 307200 \cdot T_s = 10\,\text{ms}$ long and consists of 20 slots of length $T_{slot} = 15360 \cdot T_s = 0.5\,\text{ms}$, numbered from 0 to 19. A subframe is defined as two consecutive slots where subframe i consists of slots $2i$ and $2i+1$. For FDD, 10 subframes are available for downlink transmission and 10 subframes are available for uplink transmissions in each 10 ms interval. Uplink and downlink transmissions are separated in the frequency domain. In half-duplex FDD operation, the UE (User Equipment) cannot transmit and receive at the same time while there are no such restrictions in full-duplex FDD.

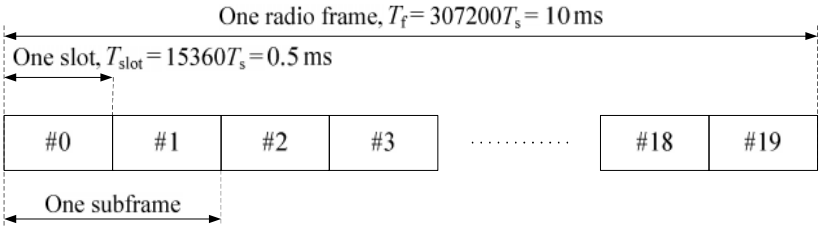

Figure 1Frame structure type 1.

This paper is organized as follows: Section 2 discusses about the LTE Physical downlink channels and their functions. Section 3 describes the system model of transmitter and receiver for the Physical downlink channels based on 3GPP specifications. Section 4 discusses the proposed architecture for the SISO, MISO and MIMO transmitters and receivers. Section 5 gives the simulated and implemented results for the proposed system of transmitter and receiver. Finally this paper is concluded with section 6.

2. LTE PHYSICAL DOWNLINK CHANNELS

The LTE downlink physical channels include three control channels and three data channels. The control channels PDCCH (Physical Downlink Control Channel), PCFICH (Physical Control Format Indicator Channel) and PHICH (Physical Hybrid Indicator Channel) are essential for the successful reception, demodulation and decoding of the data channels PDSCH **(**Physical Downlink Shared Channel**)**, PBCH (Physical Broadcast Channel) and PMCH (Physical Multicast Channel). The signals for the control channels are transmitted at the start of each subframe in a LTE grid.

The PDSCH (Physical Downlink Shared Channel) is the main data-bearing downlink channel in LTE. It is used for all user data, as well as for broadcast system information which is not carried on the PBCH, and for paging messages – there is no specific physical layer paging channel in the LTE system. The PDSCH is utilized basically for data and multimedia transport. [1] The PBCH (Physical Broadcast Channel) carries the basic system information which allows the other channels to be configured and operated in the LTE grid. PBCH information is divided into two categories. They are Master Information Block (MIB) and System Information Block (SIB). QPSK is the only modulation used [1]. The PMCH (Physical Multicast channel) physical channel structure is defined for future use. MBMS enables a set of eNBs to transfer information simultaneously for a given duration. MBFSN appears to UE (User Equipment) as a transmission from a single large cell and improves the signal-to-interference noise ratio. Since the operation of data transmission is different from that of MBFSN, UE should have a separate channel estimate for MBSFN reception; therefore normal reference signal is not mixed with the MBSFN reference

signal in the same subframe and transmission of PDSCH and PMCH in the same subframe is not possible [1].

The PDCCH (Physical Downlink Control Channel) is to carry mainly scheduling information of different types such as Downlink resource scheduling, Uplink power control instructions. The control information carried by PDCCH is DCI (Downlink Control Information) which is transmitted as an aggregation of Control Channel Elements (CCEs). Each CCE consists of 9 Resource Element Groups (REGs) and each REG has 4 resource elements (Res). Each RE carries 2 bits. A PDCCH can transmit 1, 2, 4 or 8 CCEs. QPSK is the only available modulation format. [2]The PCFICH is transmitted on the first symbol of every sub-frame and carries a Control Format Indicator (CFI) field. The CFI contains a 32 bit code word that represents 1, 2, 3 or 4. CFI-4 is meant for future use [2]. The value of the PCFICH informs the UE (User Equipment) about the number of OFDM symbols used for the transmission of control channel (PDCCH) information in a subframe. The PCFICH uses QPSK modulation. The PHICH channel is used to report the Hybrid ARQ (Hybrid Automatic Repeat Request) status which indicates to the UE whether the uplink user data is correctly received or not. The HARQ indicator is 1 bit long - "0" indicates ACK, and "1" indicates NACK. BPSK modulation is used in PHICH channel. [3]

3. SYSTEM MODEL

In LTE, the data which is given to the transmitter should experience the following channel processing steps. Figure 2 shows the channel processing steps of transmitter. Figure 3 shows the channel processing steps of receiver.

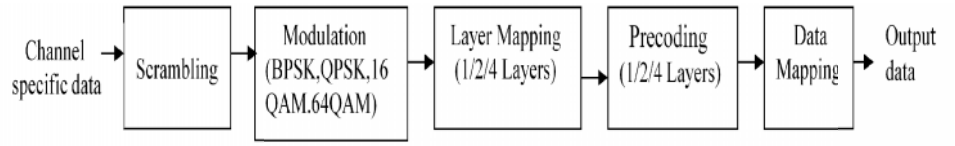

Figure 2 Modules of Transmitter

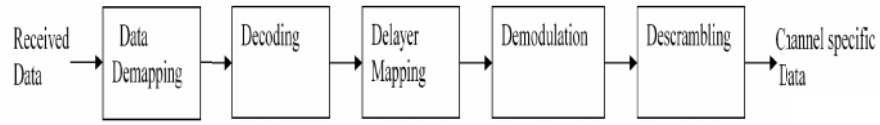

Figure 3 Modules of Receiver

3.1 CHANNEL PROCESSING STEPS OF TRANSMITTER

3.1.1 Scrambling

For each codeword q, the block of bits $b^{(q)}(0),...,b^{(q)}(M_{bit}^{(q)}-1)$, where $M_{bit}^{(q)}$ is the number of bits in codeword q transmitted on the physical channel in one subframe, shall be scrambled according to (1) for all the five channels except PHICH, where $c^{(q)}(i)$ is a Gold sequence of length "i". The modulation and scrambling of PHICH is done according to (2) [4].

$$\tilde{b}^{(q)}(i) = \left(b^{(q)}(i) + c^{(q)}(i)\right) \bmod 2 \qquad \text{..... (1)}$$

$$d(i) = w\left(i \bmod N_{\mathrm{SF}}^{\mathrm{PHICH}}\right) \cdot (1 - 2c(i)) \cdot z\left(\left\lfloor i / N_{\mathrm{SF}}^{\mathrm{PHICH}} \right\rfloor\right)$$
$$i = 0,.....M_{symb} - 1 \qquad \text{..... (2)}$$

Where $M_{\mathrm{symb}} = N_{\mathrm{SF}}^{\mathrm{PHICH}} \cdot M_{\mathrm{s}}$ and $N_{\mathrm{SF}}^{\mathrm{PHICH}} = \begin{cases} 4 & \text{normal cyclic prefix} \\ 2 & \text{extended cyclic prefix} \end{cases}$

3.1.2 Modulation

In general LTE follows four different types of modulation techniques such as BPSK, QPSK, 16 QAM and 64 QAM. The physical downlink channels and their corresponding modulation techniques are shown in Table 1.

Table 1 Channel and Modulations

Channels	Type of Modulation
PBCH,PCFICH,PDCCH	QPSK
PDSCH	QPSK, 16 QAM, 64 QAM
PMCH	QPSK, 16 QAM, 64 QAM
PHICH	BPSK

The scrambled sequence is then modulated to create a block of complex valued modulated symbols as $d^{(q)}(0),...,d^{(q)}(M_{\mathrm{symb}}^{(q)} - 1)$. In QPSK modulation a pairs of bits are mapped to complex valued modulation symbols I+ jQ, as shown in Table 2. Similarly the distributed arithmetic processing is applied for 16QAM, 64QAM [4].

Table 2 QPSK Modulation

b(i),b(i+1)	I	Q
00	$1/\sqrt{2}$	$1/\sqrt{2}$
01	$1/\sqrt{2}$	$-1/\sqrt{2}$
10	$-1/\sqrt{2}$	$1/\sqrt{2}$
11	$-1/\sqrt{2}$	$-1/\sqrt{2}$

3.1.3 Layer Mapping

The modulated symbols are then layer mapped to one or more layers depending upon the number of antenna ports selected .The complex modulated input symbols are layer mapped as $x(i) = \left[x^{(0)}(i) \quad ... \quad x^{(\upsilon-1)}(i)\right]^T$, $i = 0,1,...,M_{\mathrm{symb}}^{\mathrm{layer}} - 1$ where υ is the number of layers and $M_{\mathrm{symb}}^{\mathrm{layer}}$ is the number of modulation symbols per layer in the layer mapping module.In this paper, transmitter diversity is adopted; the input symbols are mapped to layers according to Table 3 [4].

Table 3 Mapping to layers

Number of layers	Layer mapping i=0,1,..., M^{layer}_{symb}-1
1	$X^{(0)}(i)=d^{(0)}(i)$
2	$X^{(0)}(i)=d^{(0)}(2i)$ $M^{layer}_{symb}=M^{(0)}_{symb}/2$ $X^{(1)}(i)=d^{(0)}(2i+1)$
4	$X^{(0)}(i)=d^{(0)}(4i)$ $X^{(1)}(i)=d^{(0)}(4i+1)$ $X^{(2)}(i)=d^{(0)}(4i+2)$ $M^{layer}_{symb}=M^{(0)}_{symb}/4$ $X^{(3)}(i)=d^{(0)}(4i+3)$

3.1.4 Precoding

The precoder takes a block from the layer mapper $x^{(0)}(i)$, $x^{(1)}(i)$,... $x^{(v-1)}(i)$, and generates a sequence for each antenna port $y^{(p)}(i)$, p is the transmit antenna port number and is {0},{0,1} or {0,1,2,3}[4]. For transmission over a single antenna, port processing is carried out by (3).

$$y^{(p)}(i) = x^{(0)}(i) \quad \ldots . (3)$$

Precoding for transmit diversity is available on two or four antenna ports. In two antenna port precoding, an Alamouti scheme is used for precoding. This precoding procedure for two antenna case is defined by (4)

$$\begin{bmatrix} y^{(0)}(2i) \\ y^{(1)}(2i) \\ y^{(0)}(2i+1) \\ y^{(1)}(2i+1) \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & j & 0 \\ 0 & -1 & 0 & j \\ 0 & 1 & 0 & j \\ 1 & 0 & -j & 0 \end{bmatrix} \begin{bmatrix} \mathrm{Re}\left(x^{(0)}(i)\right) \\ \mathrm{Re}\left(x^{(1)}(i)\right) \\ \mathrm{Im}\left(x^{(0)}(i)\right) \\ \mathrm{Im}\left(x^{(1)}(i)\right) \end{bmatrix} \quad \ldots\ldots (4)$$

with $i = 0,1,\ldots,M^{\text{layer}}_{\text{symb}}-1$ with $M^{\text{ap}}_{\text{symb}} = 2M^{\text{layer}}_{\text{symb}}$. For transmission on four antenna ports, $p \in \{0,1,2,3\}$, the output $y(i) = \left[y^{(0)}(i) \quad y^{(1)}(i) \quad y^{(2)}(i) \quad y^{(3)}(i)\right]^T$, $i = 0,1,\ldots,M^{\text{ap}}_{\text{symb}}-1$ of the precoding operation is defined by (5)

$$\begin{bmatrix} y^{(0)}(4i) \\ y^{(1)}(4i) \\ y^{(2)}(4i) \\ y^{(3)}(4i) \\ y^{(0)}(4i+1) \\ y^{(1)}(4i+1) \\ y^{(2)}(4i+1) \\ y^{(3)}(4i+1) \\ y^{(0)}(4i+2) \\ y^{(1)}(4i+2) \\ y^{(2)}(4i+2) \\ y^{(3)}(4i+2) \\ y^{(0)}(4i+3) \\ y^{(1)}(4i+3) \\ y^{(2)}(4i+3) \\ y^{(3)}(4i+3) \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & 0 & 0 & j & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & j & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & j & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & -j & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & j & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & j \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & j \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & -j & 0 \end{bmatrix} \begin{bmatrix} \mathrm{Re}\left(x^{(0)}(i)\right) \\ \mathrm{Re}\left(x^{(1)}(i)\right) \\ \mathrm{Re}\left(x^{(2)}(i)\right) \\ \mathrm{Re}\left(x^{(3)}(i)\right) \\ \mathrm{Im}\left(x^{(0)}(i)\right) \\ \mathrm{Im}\left(x^{(1)}(i)\right) \\ \mathrm{Im}\left(x^{(2)}(i)\right) \\ \mathrm{Im}\left(x^{(3)}(i)\right) \end{bmatrix} \quad \ldots\ldots (5)$$

with $M_{\text{symb}}^{\text{ap}} = \begin{cases} 4M_{\text{symb}}^{\text{layer}} & \text{if } M_{\text{symb}}^{(0)} \bmod 4 = 0 \\ \left(4M_{\text{symb}}^{\text{layer}}\right) - 2 & \text{if } M_{\text{symb}}^{(0)} \bmod 4 \neq 0 \end{cases}$.

3.1.5 Mapping to Resource Elements

For each of the antenna ports used for transmission of the physical channel, the block of complex-valued symbols $y^{(p)}(0),...,y^{(p)}(M_{\text{symb}}^{\text{ap}}-1)$ shall be mapped in sequence starting with $y^{(p)}(0)$ to resource elements (k,l) , where 'k' represents the rows of the LTE grid and 'l' represents the columns of the LTE grid. The downlink channels' precoded symbols are mapped to the LTE grid in their respective resource element groups (REG), and control channels are mapped only in the first OFDM symbol of each subframe and are transmitted.

3.2 CHANNEL PROCESSING STEPS OF RECEIVER

3.2.1 Demapping From Resource Elements

While data is received on the antenna ports, the block of complex-valued symbols $y^{(p)}(0),...,y^{(p)}(M_{\text{symb}}^{\text{ap}}-1)$ shall be demapped in sequence starting with $y^{(p)}(0)$ from resource elements (k,l) [4].

3.2.2 Decoding

The decoder takes as input a block of vectors $y(i) = \left[... \quad y^{(p)}(i) \quad ...\right]^T$, $i = 0,1,...,M_{\text{symb}}^{\text{ap}}-1$ demapped from resources on each of the antenna ports, where $y^{(p)}(i)$ represents the signal from antenna port p and generates a block of vectors $x(i) = \left[x^{(0)}(i) \quad ... \quad x^{(\upsilon-1)}(i)\right]^T$, $i = 0,1,...,M_{\text{symb}}^{\text{layer}}-1$ for the delayer mapping. For reception on a single antenna port, decoding is defined by (6) [4].

$$x^{(0)}(i) = y^{(p)}(i) \qquad \text{... (6)}$$

Similarly for reception on two antenna ports the reverse operation of (4) is performed.

3.2.3 Delayer Mapping

The complex-valued symbols for each of the code words to be received are delayer mapped from one or several layers. Complex-valued symbols $d^{(q)}(0),...,d^{(q)}(M_{\text{symb}}^{(q)}-1)$ for codeword q shall be demapped from the layers $x(i) = \left[x^{(0)}(i) \quad ... \quad x^{(\upsilon-1)}(i)\right]^T$, $i = 0,1,...,M_{\text{symb}}^{\text{layer}}-1$ where υ is the number of layers and $M_{\text{symb}}^{\text{layer}}$ is the number of symbols per layer. For a single antenna port, a single layer is used, and the delayer mapping is defined by (7) [4].

$$d^{(0)}(i) = x^{(0)}(i) \qquad \text{... (7)}$$

Similarly for two antenna ports the operations performed in Table 3 are reversed, and the two layers are delayer mapped into a single layer.

3.2.4 Demodulation

The complex-valued symbols $d^{(q)}(0),...,d^{(q)}(M_{\text{symb}}^{(q)}-1)$ of code word q, shall be demodulated using a demodulation scheme which is reverse of transmitter, resulting in a block of bits $\tilde{b}^{(q)}(0),...,\tilde{b}^{(q)}(M_{\text{bit}}^{(q)}-1)$

3.2.5 Descrambling

The demodulated symbols in a code word q, after descrambling results in the block of bits $b^{(q)}(0),...,b^{(q)}(M_{\text{bit}}^{(q)}-1)$, where $M_{\text{bit}}^{(q)}$ is the number of bits in code word q received on each control channels in one sub frame. The descrambling is defined according to (8).

$$b^{(q)}(i) = \left(\tilde{b}^{(q)}(i) + c^{(q)}(i)\right) mod 2 \qquad \text{..... (8)}$$

where $c^{(q)}(i)$ is the generated pseudo random Gold sequence. The descrambling sequence is initialized with same values as that of the transmitter at start of each subframe.

4. PROPOSED ARCHITECTURE OF PHYSICAL DOWNLINK CHANNELS FOR LTE

4.1 TRANSMITTER ARCHITECTURE

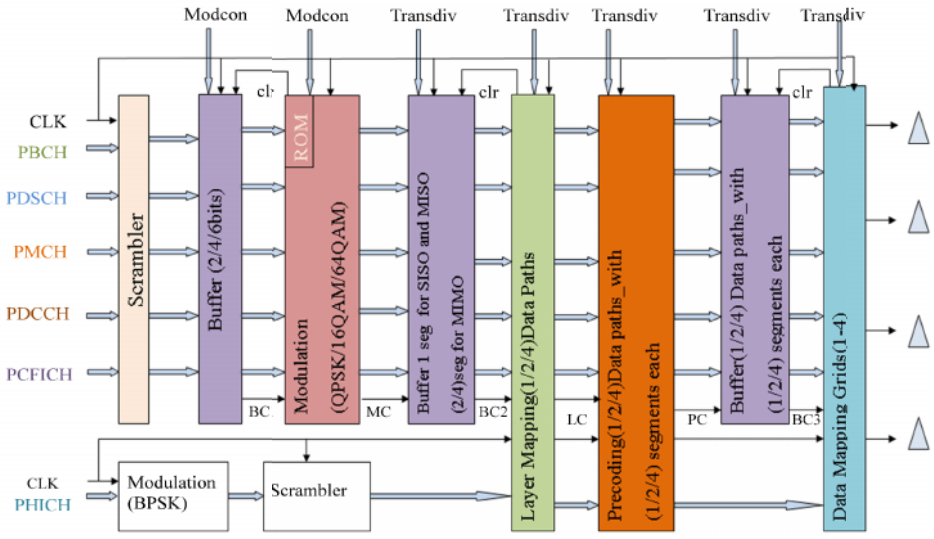

Figure 4 Pipelined Buffer Controlled Architecture of Transmitter for downlink Channels in LTE

The reason for going to pipelined architecture is to reduce the critical path delay which can be exploited to increase the clock speed or to reduce the power consumption for the same speed. In this pipelined buffer control architecture, the different processing modules are segregated to segments and they have buffers in between them to work independently .This reduces the critical path as a whole when compared with buffer less segmented approach. The buffer control is used

to synchronize all the segments and send the information out to the grid.Figure 4 explains the pipelined buffer controlled architecture for the transmitter. The transmitter side of the architecture consists of Scrambling, Modulation, Layer Mapping, Precoding and Mapping to the Resource Elements .In addition to these buffers are included in this architecture.

The scrambler generates scrambling bits at the rate of one bit for every clock cycle. For the PHICH channel the one bit input either 0 (indicating ACK) or 1 (indicating NACK) is first modulated using BPSK modulation and then scrambled. The modulation mapper takes 2bits /4bits/ 6bits for QPSK/16QAM/64QAM modulations respectively as inputs. Hence a buffer is included before the modulation block. The task of the buffer is to store either 2bits/4bits/6bits in two clock cycles or four clock cycles or six clock cycles based on the type of modulation given to it by the variable "Modcon". After the corresponding bits have been stored, the buffer will send a buffer control signal indicated by the variable "BC1" to the modulation block. For every possible pair of 2 bits/4 bits/6 bits i.e., "00" to "11" /"0000" to "1111"/ "000000" to "111111", there resides a corresponding modulated value (16 bits) stored in the modulation mapper. All the modulation mapper has to do is, check the variable "Modcon" for the type of modulation given and simply maps the incoming bits to the correct segment of modulated data. The output of modulation mapper is 16 bits for every clock cycle which will be represented as a segment in the following sections. The modulation block after performing the modulation sends a clear signal denoted as "clr" to the buffer indicating the buffer to send the next stream of bits based on the "Modcon". The layer mapping module simply maps the modulated bits (i.e. segment) into 1/2/4 layers depending on the transmitter diversity (SISO, MISO and MIMO) indicated by "Transdiv" variable. For the single antenna (1x1) the layer mapper maps every single segment of the modulator to the first layer/data path of all the physical downlink channels. In case of MISO (2x1 and 4x1) every single segment is mapped into 2 layers and four layers respectively. In case of MIMO (2x2 and 4x2) two different segments are mapped to two layers (one segment in each layer) and 4 different segments are mapped to 4 layers respectively.

To achieve this kind of mapping in the respective layers, a buffer is included in front of the layer mapper. For the SISO and MISO concepts, the buffer will wait for one clock cycle to store a single segment. For the 2x2 MIMO the buffer will wait for two clock cycles to store the two different segments and for the 4x2 MIMO the buffer will wait for four clock cycles to store four different segments. After storing the respective segments, the buffer will send a buffer control signal "BC2" to the layer mapper. The layer mapper after performing the mapping operations sends a "clr" signal to the buffer signalling it to send the next set of segments. The precoding block adds parity bits to the segments by appending zeros and conjugates of original data. The transmitter diversity "Transdiv" configures the precoding block also. When the transmitter diversity is SISO or MISO the 1/2/4 data paths consists of the same single segment. They are precoded as such. When the transmitter diversity is MIMO two different cases exists, 2x2 and 4x2.The single segment in every layer is precoded into two segments for 2 layers and precoded into 4 segments for 4 layers. This all happens in a single clock cycle. The Resource element mapper only maps a single segment at a clock cycle to the resource elements. The buffer in front of the RE mapper stores the (1/2/4) segments in 1/2/4 data paths and delivers a segment for every clock cycle to the LTE grid.

Table 4 Total Delays experienced

Transmitter Diversity	Representation	Modulation	Delays (in CLK)
SISO (1X1)/ MISO 2X1)/ MISO(4X1)	001/011 / 101	BPSK QPSK 16QAM 64QAM	14/14/14 6/7/9 8/9/11 10/11/13
MIMO2X2	100	BPSK QPSK 16QAM 64QAM	14 CLK 10 CLK 12 CLK 14 CLK
MIMO 4X2	110	BPSK QPSK 16QAM 64QAM	14 CLK 16 CLK 27 CLK 37 CLK

4.2 RECEIVER ARCHITECTURE

The receiver side of the architecture consists of Demapping from the Resource Elements, Decoding and Detection, Delayer Mapping and Descrambling as shown by the Figure 5.The receiver architecture is designed with two receiving antennas. When the transmitter diversity is SISO (1x1) or MISO (2x1 and 4x1) antenna 1 is enabled to receive. Similarly when MIMO (2x2 and 4x2) case occurs both the antennas are enabled to receive. The data demapper module demaps the segments from the resource elements.

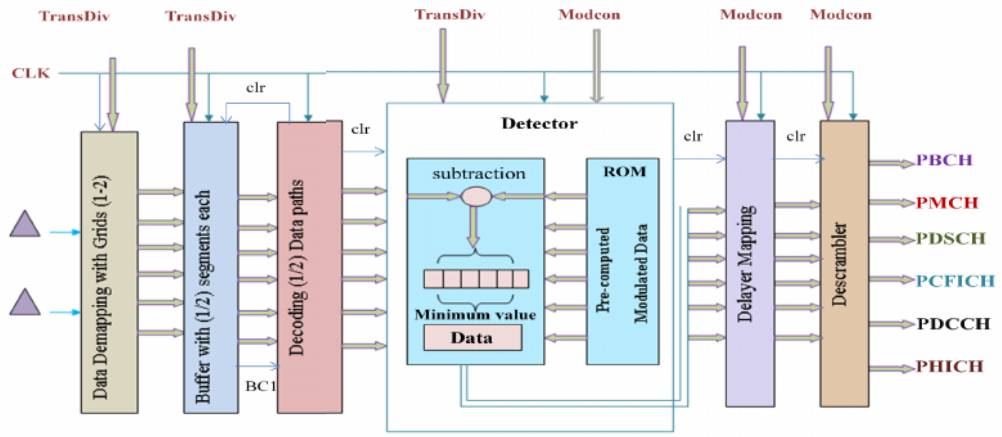

Figure 5 Pipelined Buffer Controlled Architecture of Receiver for downlink Channels in LTE

For the SISO and MISO cases there is only one segment. The buffer stores the single segment in a clock cycle. When it is MIMO the buffer waits for two clock cycles and stores the two segments and sends the buffer control signal (BC1) , signalling the decoding module to accept the segments in the next clock cycle. The decoding module removes the parity bits i.e. the extra padded zeros and conjugate bits in the next clock cycle and sends the clear signal represented as “clr” to the buffer and the detector modules.

The detector consists of precomputed modulated data stored in it and a comparator. Initially after the reception of "clr" signal from the decoder, the received data and the precomputed data are subtracted and the results are compared with each other to find the minimum distance value using the Alamouti scheme. Once the comparisons are done and the output is generated the detector sends its clear signal to the delayer mapping module. Thus the detected or demodulated output is 2 bits/4 bits/6 bits for QPSK/16QAM/64QAM modulations respectively for each layer. This process goes for every clock cycle. The delayer mapping module delayers the two layers of MIMO into a single layer thus comprising 4 bits/8 bits/12 bits depending on the Modcon (modulation) input variable given and sends the clear signal. This all occurs in a single clock cycle. Since SISO comes in a single layer, there is no need of delayer mapping. The descrambling is performed by XORing the input bits with the Gold sequence used in the transmitter and produces 1 bit (ACK/NACK) for PHICH and 2 bits/4 bits/6 bits depending on the "Modcon" for the remaining channels in a single clock cycle. Thus the data and control messages are retrieved in the receiver.

5. RESULTS AND DISCUSSIONS

5.1 Simulation output for SISO transmitter

The SISO transmitter for PBCH channel is shown in Figure 6. The output of bit scrambler, the first module of transmitter "scr_pbch" is a single bit for every clock cycle and it's own clock canc_pbch is shown below. The buffer indicated by "buffscr2pbch" in the figure 4 wait for two clock cycles and got the pair of bits from scrambler. The modulation will be performed in the next clock cycle. The modulated segment "mod_pbch" is layer mapped into a single layer, precoded and data mapped in the forth coming clock cycles with a delay of one clock cycle between each process. The precoded data shown as "prelayer1pbch" for transmit antenna 1 is mapped into the corresponding resource element for the PBCH channel in the LTE grid in the next clock cycle. Therefore the SISO transmitter for PBCH takes a total delay of 6 clock cycles. This explanation suits well for the PDSCH, PMCH, PDCCH and PCFICH channels.

Figure 7 and 8 describe the SISO transmitter for PDSCH [16QAM] and PDSCH [64QAM] respectively. The buffer represented as "buffscr246pdsch" will wait for 4 clock cycles and 6 clock cycles before sending 4 bits and 6 bits to the modulation mapper respectively. The delays required for remaining modules are similar to PBCH (SISO). Therefore the PDSCH channel takes a total delay of 8 clock cycles for 16QAM and 10 clock cycles for 64QAM modulations.

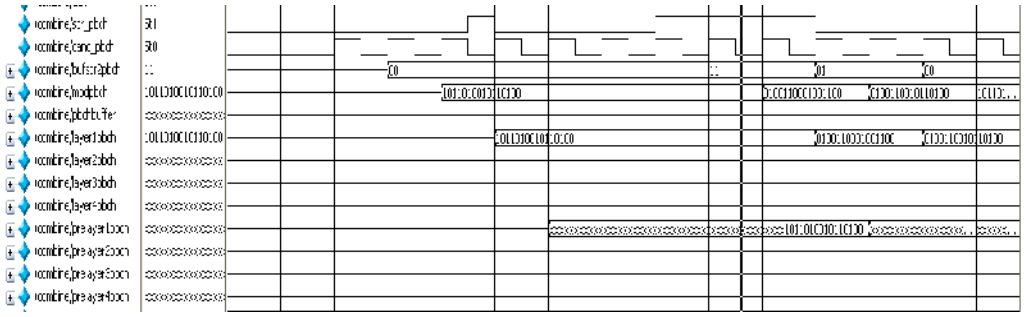

Figure 6 Simulation result for SISO transmitter (1X1) PBCH

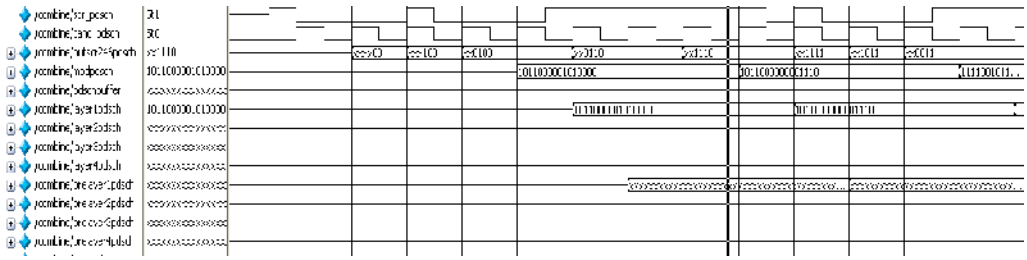

Figure 7 Simulation result for SISO transmitter (1X1) PDSCH [16QAM]

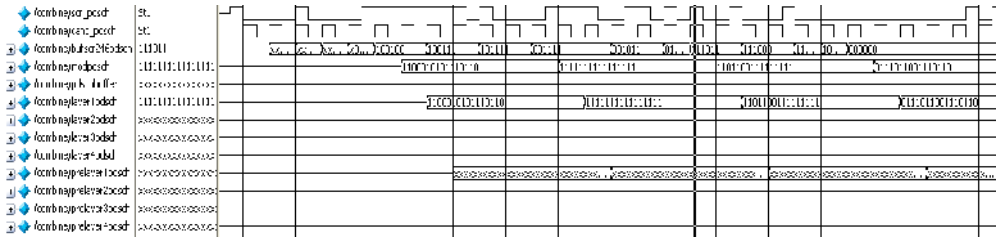

Figure 8 Simulation output for SISO transmitter-PDSCH [64QAM]

The SISO transmitter for PHICH is shown in Figure 9. The first step is a modulation instead of scrambling, in which a single bit input whether 0 (ACK) or 1(NACK) is BPSK modulated. Then the modulated bits are scrambled to produce a output of 12 segments (192 bits) represented as "out" in the figure 9.The layer mapping and precoding are done in the next occurring clock cycles. The data mapping module takes 12 clock cycles to map the 12 PHICH segments to the transmitter antenna 1.Therefore total delay is 14 clock cycles.

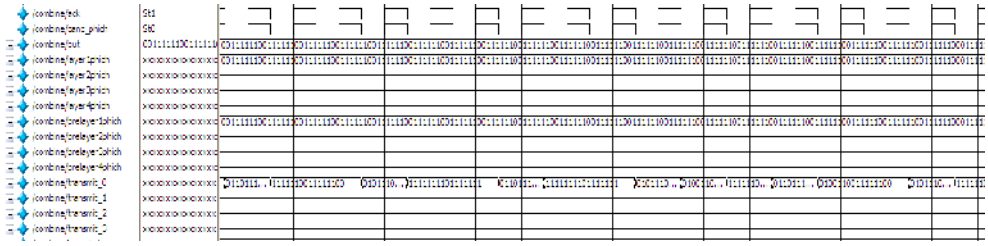

Figure 9 Simulation output for SISO transmitter-PHICH

5.2 Simulation output for MISO (2x1) transmitter

The MISO (2x1) transmitter for PDCCH channel is shown in Figure 10. It is similar to SISO except that the modulation mapper's output "modpdcch" is layer mapped into two layers represented as "layer1pbch" and "layer2pdcch". The single segment in each of the two layers is precoded into two segments represented as "prelayer1pdcch" and "prelayer2pdcch", The data mapper module for the transmit antenna 1 and 2 maps the two segments into their LTE grids in two clock cycles. Therefore the total delay is 7 clock cycles. This explanation suits well for the PDSCH [QPSK], PMCH, PBCH and PCFICH channel. PDSCH [16QAM] experiences a delay of 9 clock cycles the extra two clock cycles was being spent in waiting for 4 bits input to the modulation mapper. Also PDSCH [64QAM] experiences a delay of 11 clock cycles.

The MISO (2x1) transmitter for PHICH is shown in Figure 11. The output of the modulation mapper and scrambler module “out” consists of 12 segments which is layer mapped into 2 layers “layer1phich” and “layer2phich” as 6 segments each in the next clock cycle. The precoder module precodes these 6 segments with parity bits, giving an output of 12 segments in each data path in the next clock cycle. The data mapping module for the first two transmit antennas map the 12 segments into the resource block allocated for PHICH channel in 12 clock cycles. Therefore the total delay is 14 clock cycles. The first two antennas represented as transmit_0 and transmit_1 with the same data being transmitted for every clock cycle is shown in the Figure 11.

5.3 Simulation output for MISO (4x1) transmitter

The MISO (4x1) transmitter for PCFICH is shown in Figure 12. The processing steps and the delays experienced by the MISO (4x1) transmitter is similar to MISO (2x1) except that the layer mapping block maps the modulation output into 4 layers/data paths and the precoder precodes each segment in every layer into 4 segments. The data mapping module maps the 4 segments in 4 clock cycles. Therefore a total delay of 9 clock cycles is experienced. This explanation suits well for the PDSCH [QPPSK], PBCH and PDCCH channels. PDSCH [16QAM] experiences a total delay of 11 clock cycles. PDSCH [64QAM] experiences a total delay of 13 clock cycles.

The MISO (4x1) transmitter for PMCH [QPSK] is shown in Figure 13. The PMCH channel is only transmitted in the fourth antenna i.e.transmit_3. As it is transmitted in a single antenna, the channel processing steps of PMCH channel follows SISO strategy. Therefore the delays experienced by each module are similar to SISO transmitter. The total delay is thus 6 clock cycles. PMCH [16QAM] and PMCH [64QAM] are very much similar to the SISO transmitter PDSCH channel described earlier, therefore the total delay is 8 clock cycles and 10 clock cycles respectively. The MISO (4x1) transmitter for PHICH is shown in Figure 14. After the modulation and scrambling the 12 segments generated are layer mapped into 4 layers as such: 3 segments for each layer in the next clock cycle. The precoding module adds extra zeros and conjugates thus generating 12 segments in each of the 4 layers in the next clock cycle. The data mapping modules takes 12 clock cycles to map the precoded data into the resource blocks of 4 transmit antennas. Therefore a total delay of 14 clock cycles exists in PHICH channel.

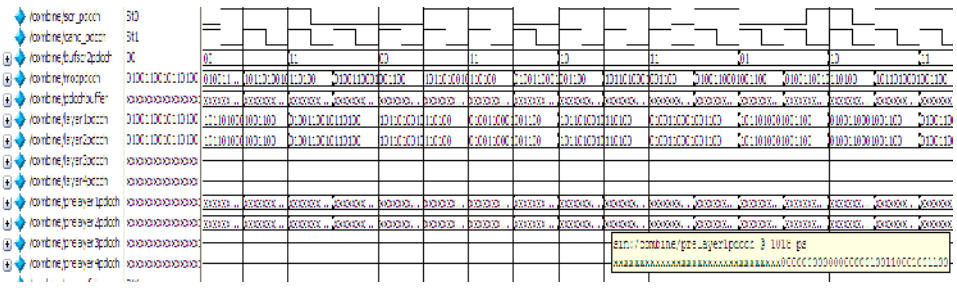

Figure 10 Simulation output for MISO (2x1) Figure transmitter-PDCCH

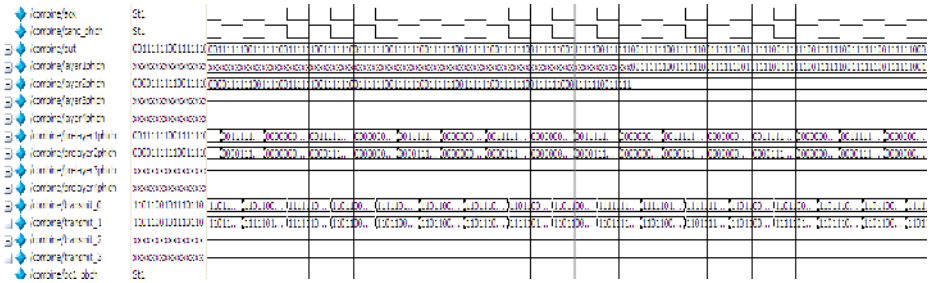

Figure 11 Simulation output for MISO (2x1) transmitter-PHICH

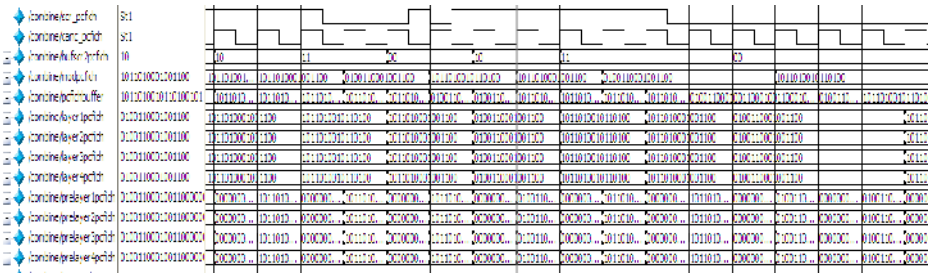

Figure 12 Simulation output for MISO (4x1) transmitter-PCFICH

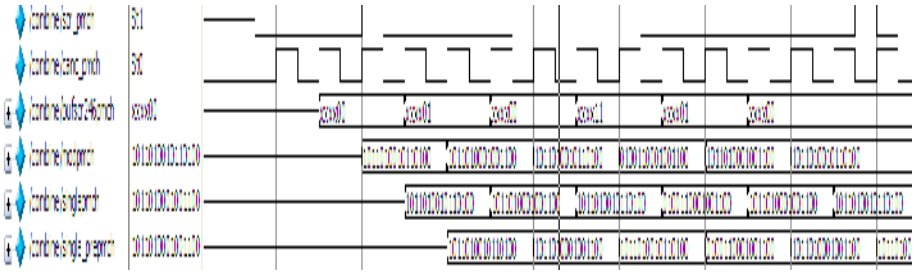

Figure 13 Simulation output for MISO (4x1) transmitter-PMCH [QPSK]

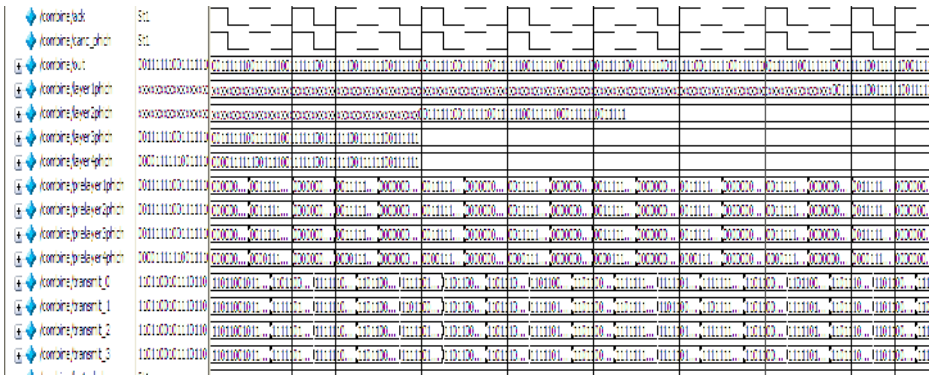

Figure 14 Simulation output for MISO (4x1) transmitter-PHICH

5.4 Simulation output for MIMO (2x2) transmitter

The MIMO (2x2) transmitter for PDSCH [QPSK] is shown in Figure 15. In MIMO (2x2), the channel processing steps and their corresponding delays are similar to MISO (2x1) upto the modulation module. The buffer represented as "pdschbuffer246" before the layer mapping module get two different segments from the modulation mapper in the sixth clock cycle. The layer mapping is done in the next clock cycle. The precoding is thus done in the 8th clock cycle generating two segments for each data path. The data mapping module takes another two clock cycles. Thus a total delay of 10 clock cycles exists. This explanation suits well for the PBCH, PDCCH and PCFICH channels. PDSCH [16QAM] experiences 12 clock cycles delay and for PDSCH [64QAM] experiences 14 clock cycles delay. The MIMO (2X2) transmitter for PHICH is similar to MISO (2x1). The transmitter outputs transmit_0 and transmit_1 carry different segments in every clock cycle.

5.5 Simulation output for MIMO (4x2) transmitter

The MIMO (4X2) transmitter for PBCH is shown in Figure 16. In MIMO (4x2), the channel processing steps and their corresponding delays are similar to MISO (4x1) up to the modulation module. In the case of MIMO (4x2), four different segments (modulation output) have to be layer mapped into the four layers/datapaths corresponding to the four transmit antennas. Hence the buffer represented as "pbchbuffer" before the layer mapping module get four different segments from the modulation mapper in the tenth clock cycle. The layer mapping is done in the next clock cycle. The precoding is thus done in the 8th clock cycle generating four segments for each data path. The data mapping module takes another four clock cycles. Thus a total delay of 16 clock cycles exists. This explanation suits well for the PDSCH, PMCH, PDCCH and PDCCH channels.

In PDSCH [16QAM] the modulation is performed in the fifth clock cycle as usual. The buffer before the layer mapping block will wait for 16 clock cycles to receive 4 different segments from the modulator and the layer mapping is performed in the 22nd clock cycle. The precoding is done in the next clock cycle. The data mapping module needs another 4 clock cycles. Thus a total delay of 27 clock cycles is experienced. In PDSCH [64QAM] the modulation is performed in the seventh clock cycle. The buffer before the layer mapper waits for 24 clock cycles to receive 4 different segments. The remaining delays in the successive modules are as such. Hence a total delay of 37 clock cycles exists. The MIMO (4X2) transmitter for PMCH is similar to MISO (4x1). The total delay is 6 clock cycles for QPSK, 7 clock cycles for 16QAM and 9 clock cycles for 64 QAM modulations.

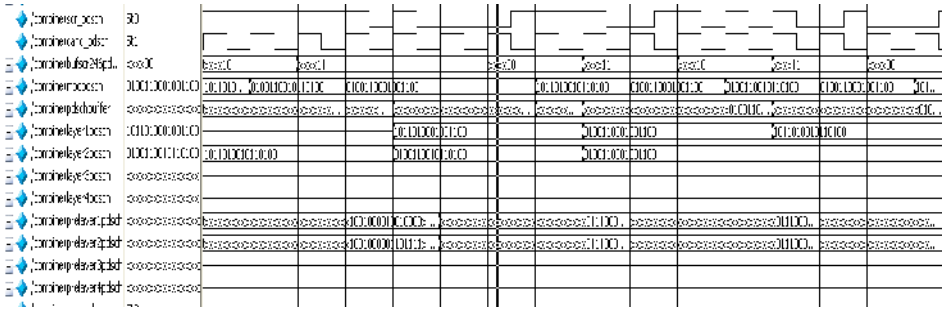

Figure 15 Simulation output for MIMO (2x2) transmitter-PDSCH [QPSK]

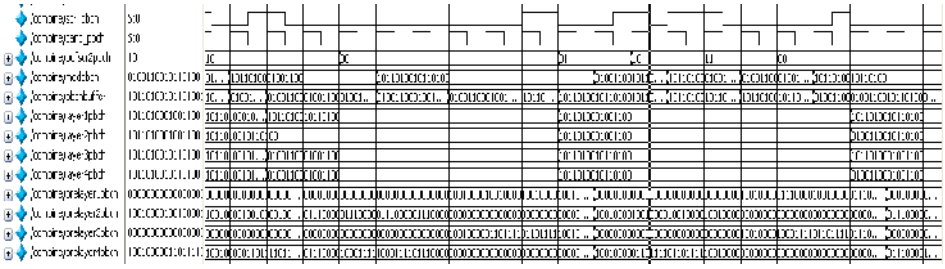

Figure 16 Simulation output for MIMO (4x2) transmitter-PBCH

5.6 Simulation output for SISO (1x1), MISO (2x1) and MISO (4x1) Receiver

The simulation results of SISO and MISO receiver for all the physical downlink channels are the same. The simulation output for SISO and MISO receiver for PBCH channel is shown in Figure 17. The output of the data demapping module of antenna 1 is “prelayer1pbch”. It is given to the decoding module in the next clock cycle. After decoding, the detector output which is 2 bits for QPSK modulation is generated in the next clock cycle. The delayer mapping and descrambling are performed in the next occurring clock cycles. The output of the descrambling module is 2 bits at a clock cycle. Therefore the total delay is 5 clock cycles. This is similar to PDCCH, PCFICH, PDSCH [QPSK] channels.

The simulation output for SISO and MISO receiver for PDSCH [16QAM] shown in Figure 18. In this case also the total delay is 5 clock cycles and the descrambler output is 4 bits at a single clock cycle. In the SISO and MISO receiver for PDSCH [64QAM] the total delay is 5 clock cycles and the descrambler output is 6 bits at a single clock cycle. The simulation output for MISO (4X1 only) receiver for PMCH [QPSK] is also similar to PDSCH. Here also the delay is 5 clock cycles with descrambler output 2 bits at a clock cycle. PMCH [16QAM] and [64QAM] also experiences 5 clock cycles delay with descrambler outputs 4bits and 6 bits respectively. The simulation output for SISO and MISO receiver for PHICH shown in Figure 19. The 12 segments are received by the data demapping module in 12 clock cycles. After that the decoding, delayer mapping, descrambling, detection and decision modules are performed in the next forthcoming clock cycles. The output of the decision module is either 0 (ACK) or 1 (NACK).Thus a total delay of 17 clock cycles occur.

5.7 Simulation output for MIMO (2x2) and MIMO (4x2)

The simulation output for MIMO (2x2 and 4x2) receiver for PDSCH [QPSK] channel shown in Figure 20. The data demapping modules of antenna 1 and 2 receives the two segments in clock cycles from the 2 antennas. Therefore the buffer has to wait for 2 clock cycles and in third clock cycle the decoder output is generated. The detector output is two bits in two data paths in the fourth clock cycle. In the fifth clock cycle the delayer mapper delayers the two layers into a single layer thus comprising 4 bits. The descrambler produces 2 bits in the sixth clock cycle. Therefore a total delay of 6 clock cycles occurs. This is similar to PDCCH, PCFICH, PBCH channels. PDSCH [16QAM] and PDSCH [64QAM] have a total delay of 6 clock cycles with 4 bits at a clock cycle in the descrambler output and 6 bits at a clock cycle in the descrambler output respectively. PMCH channel for MIMO (4x2) is similar to MISO (4x1). PHICH channel for MIMO is also similar to SISO and MISO cases.

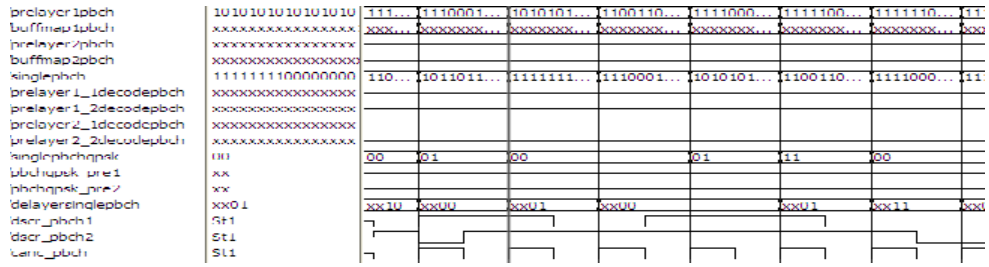

Figure 17 Simulation output for SISO and MISO receiver-PBCH

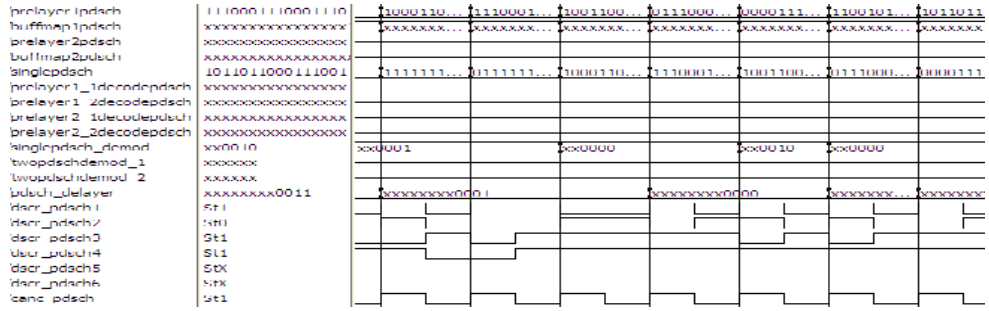

Figure 18 Simulation output for SISO and MISO receiver-PDSCH [16QAM]

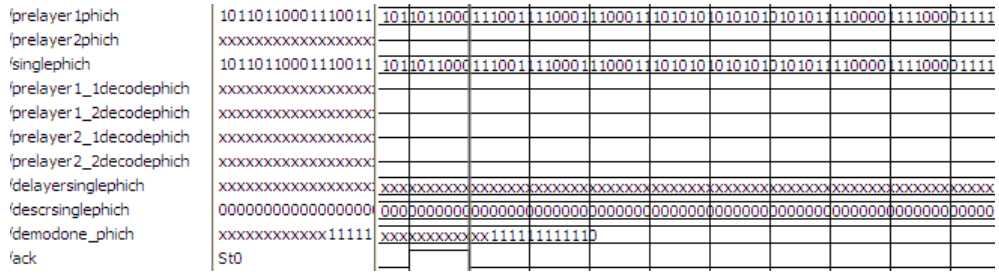

Figure 19 Simulation output for SISO and MISO receiver-PHICH

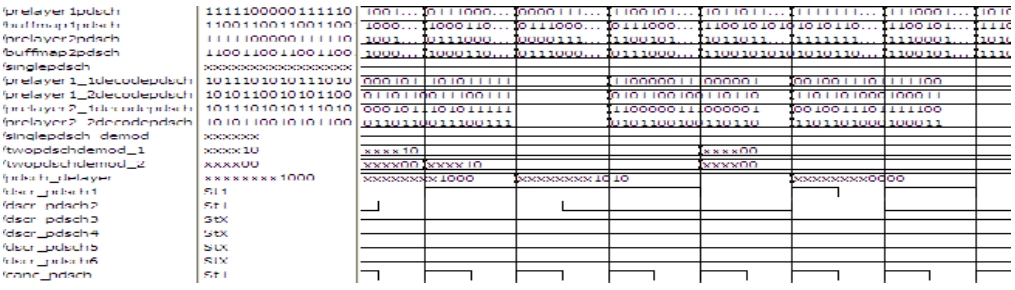

Figure 20 Simulation output for MIMO (2x2 and 4x2) receiver-PDSCH [QPSK]

5.8 Implementation Results

The RTL schematic view of the transmitter shows the input variables to each of the scrambling module, buffers, modulation, layer mapping module, precoding and data mapping modules. This is shown in Figure 21 for designer's reference. The final outputs i.e. transmit_0, transmit_1, transmit_2 and transmit_3 are also shown in the Figure 22. RTL schematic view of the receiver is shown in Figure 22. The final outputs i.e. the data and control bits are also shown for designer's reference.

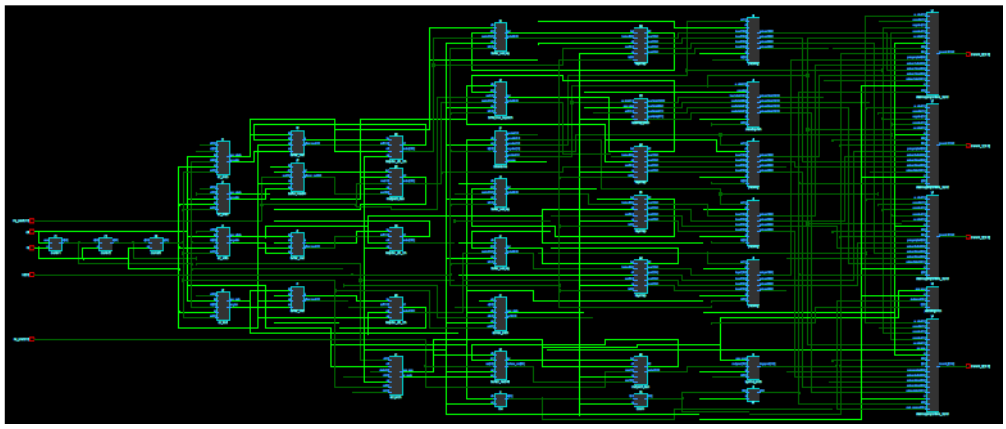

Figure 21 RTL design of Transmitter

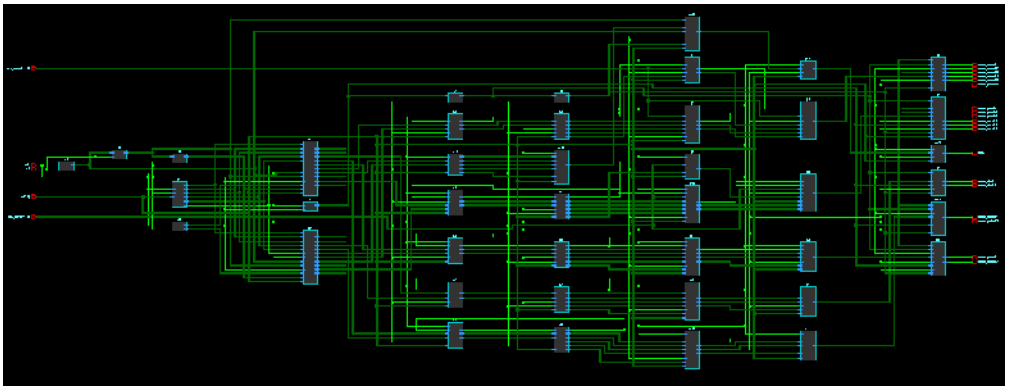

Figure 22 RTL design of Receiver

Power estimation of LTE downlink channels for transmitter and receiver is shown in Figure 23a and b. The total on chip power is 951 mW for buffer controlled architecture of transmitter. This transmitter consumes 265mW for IO, 235mW for core dynamic (clock, logic) and 452mW for device static. In core dynamic, clock signal consumes 107mW, logic signal takes 127mW. The total on chip power is 1036 mW for this receiver. This receiver consumes 20mW for IO 563mW for core dynamic (clock, logic) and 452mW for device static. In core dynamic, clock signal consumes 124mW, logic signal takes 438mW. Resource estimation of transmitter and receiver are shown in Figure 24a and b. From the graphical representation it is clear that out of the total resources about 1% is used for registers, 4% for Look up tables, 7% for the slices, 14% for the IO, 18% for BUFG. Similarly out of the total resources used for receiver, about 1% is used for registers, 23% for Look up tables, 36% for the slices, 5% for the IO, 5% for BUFG. The FPGA

framed by plan Ahead tool for transmitter and receiver are shown in Figure 25a and b. The routing between the inputs and output with available components in the chip is shown

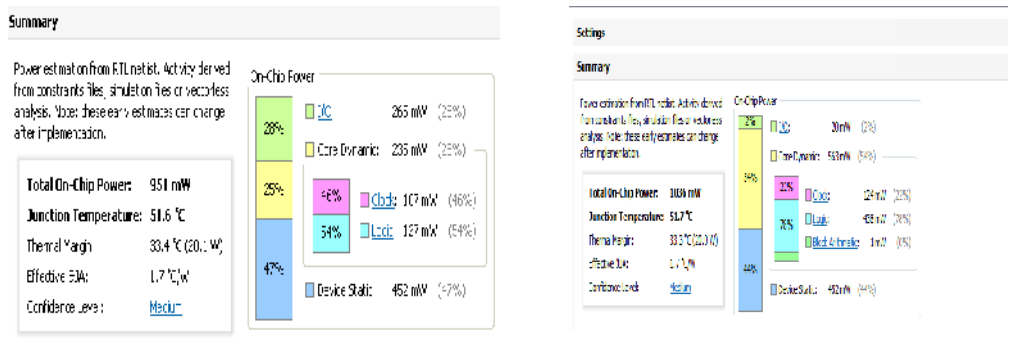

Figure 23a and 23b Power estimation of Transmitter and Receiver

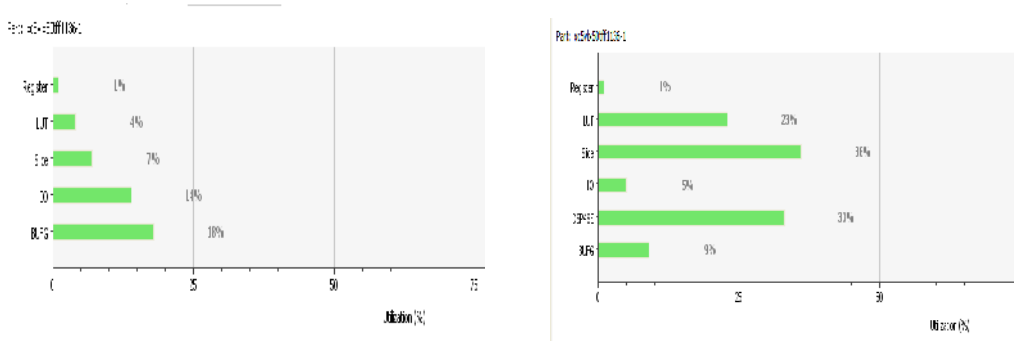

Figure 24a and 24b Resource utilization of the Transmitter and Receiver

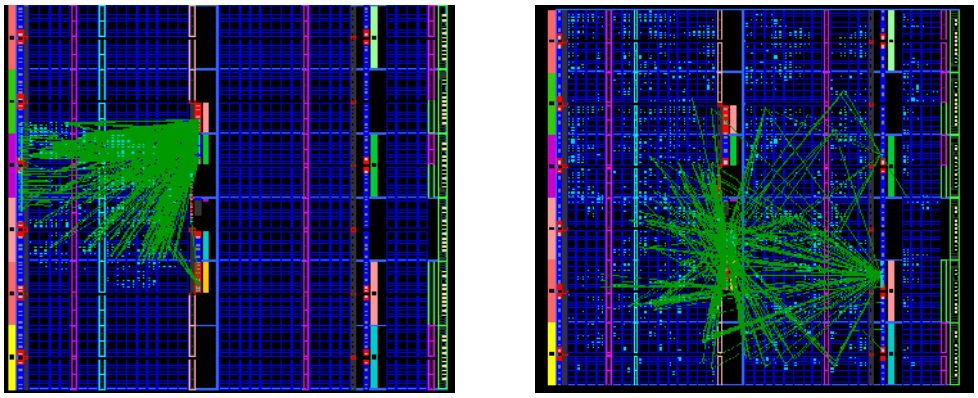

Figure 25a and 25b FPGA editor of the Transmitter and Receiver

6. CONCLUSIONS

The synthesis and implementation of pipelined buffer controlled architecture of the Single Input Single Output (SISO), Multiple Input Single Output (MISO-2x1, 4x1), and Multiple Input Multiple Output (MIMO-2x2, 4x2) transmitter and receiver for Physical Downlink Channels of LTE are thoroughly discussed in this paper. The buffers and the delays experienced by each of the modules have been explained in this architecture. The transmitter and receiver architecture for all the channels are simulated and the results are discussed. The programming was done in Verilog HDL. The simulation was done in Modelsim, synthesized using Plan Ahead 13.4 and implemented in Virtex 5 kit. Simulation results and implementation results (RTL design, power estimation, resource estimation and FPGA editor) for transmitter and receiver of LTE downlink channels are discussed. This architecture shows improvement in terms of reduced power consumption, reduced maximum delay with high speed. The pipelined buffer controlled architecture shows a minimum period of 59.334ns (nano seconds) and a maximum frequency of 16.854 MHz It maintains continuity between the modules. Also the formation of junk data between the modules is avoided by the use of “BC” and “clr” signals.

ACKNOWLEDGEMENT

The authors wish to express their sincere thanks to All India Council for Technical Education, New Delhi for the grant to do the project titled Design of Testbed for the Development of Optimized Architectures of MIMO Signal Processing (No: 8023/RID/RPS/039/11/12) .They are also thankful to the Management and Principal of Mepco Schlenk Engineering College, Sivakasi for their constant support and encouragement to carry out this part of the project work successfully.

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