

## Call for Papers

**Special Issue on: "3-D Network-on-Chip Architectures and Design Methodologies"**

### Guest Editors:

MOHAMMAD AYOUB KHAN ,  
Centre for Development of Advanced Computing(C-DAC)  
Ministry of Communications and IT, Government of India  
B-30, Sector 62, NOIDA, India

ABDUL QUAIYUM ANSARI  
Department of Electrical Engineering  
Jamia Millia Islamia (A central Government University)  
New Delhi-25, India

### Introduction

Network-on-Chip (NoC) is a communication paradigm for large VLSI systems implemented on a single silicon chip. This uses as a new approach to design complex System-on-a-chip (SoCs). The NoC-based systems can accommodate multiple complex (heterogeneous) SoC designs. In any NoC system, cores such as processor, memories, and specialized IP blocks exchange data using a protocol and physical infrastructure of on-chip networks. The conventional two-dimensional (2-D) integrated circuit (IC) has limited scope for floor planning and therefore limits the performance improvements resulting from the Network-on-Chip (NoC) paradigm. Three Dimensional (3-D) ICs are able to obtain significant performance benefits over 2-D ICs based on the electrical and mechanical properties resulting from the new geometrical arrangement (topology). The arrangement of 3-D also offers opportunities for new circuit architecture based on the geometric capacity that provide greater numbers of interconnections among multi-layer active circuits. The emerging 3-D VLSI Integration and process technologies allow the new design opportunities in 3-D NoC. The 3-D NoC can reduce significant amount of wire length for local and global interconnects.

### Subject Coverage

- Emerging topologies and architecture synthesis for 3-D NoC
- Routing algorithm and micro architecture of 3-D NoC
- Memory Architecture for NoC
- Power and Energy issues in 3-D NoC
- Dynamic on-Chip reconfiguration in 3-D NoC
- 3-D Network simulator
- Verification, debug and testing strategies for of 3-D NoC
- Performance and power estimation techniques
- Emerging technologies and new communication paradigms
- Clockless 3-D NoC architectures and asynchronous communication techniques
- Reliability issues in 3-D NoC
- QoS Parameters in 3-D NoC
- Emerging technologies for NoCs (Optics, CNFET, Nanowires)

## **IMPORTANT DATES**

Submission Deadline : September 15, 2011  
Authors Notification : October 2, 2011  
Final Manuscript Due : October 30, 2011  
Publication Dates : Determined by the Editor-in-Chief

## **Submission Instructions**

Papers must not have been published, accepted for publication, or presently be under consideration for publication elsewhere. The standard peer review process will be used to select papers for the special issue. Electronic submission in PDF format must be made in the standard of AIRCC format. Accepted papers must follow the guidelines posted at: [http://airccse.org/journal/aircc\\_template.doc](http://airccse.org/journal/aircc_template.doc) to format the final papers.

The authors must submit their papers to special Issue on or before the submission due date of **September 15, 2011**. Papers must be sent to: [sivlics@airccj.org](mailto:sivlics@airccj.org) / [secretary@airccse.org](mailto:secretary@airccse.org).